JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATIONS-APRIL 2025

B.Tech-VI Semester (ECE)

COURSE CODE (CREDITS): 18B1WEC744 (3) MAX. MARKS: 25

COURSE NAME: FPGA based Instrumentation System Design

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 1.5 Hours

Note: *(a) All questions are compulsory. (b) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems.*

Q. No	Question	CO	Marks
Q1	*'Arrays are different from register vectors'* is this statement appropriate or not? Justify with proper description along with suitable example of each of these.	CO-2	2
Q2	Defparam and localparam are the two important keywords of Verilog HDL. How are these two different from each other?	CO-2	1.5

Q3	What would be the output/effect of the following statements?
	a) latch=4'd12;
	$display("the current value of latch=%b\n", latch);
	b) in_reg=3'd2;
	$monitor($time, "In register value=%b\n", in_reg[2:0]);
	c) 'define MEM_SIZE 1024
	$display("The maximum memory size is %h", MEM_SIZE);
		CO-2	1.5

Q4	What are the basic components of a module? Explain each one of them. Which components are mandatory?	CO-2	2
Q5	Why the ports of type *input* and *inout* cannot be declared as *reg*? Discuss with suitable justification.	CO-2	1.5
Q6	An 8:1 multiplexer has to be designed. Draw the logic diagram of the circuit for this situation. Write the gate-level modeling based Verilog design code corresponding to your logic diagram.	CO-2	1.5+3.5=5
Q7	Two signals I and J are given as input to a XOR gate. Input I is low initially, goes high at 10 units of time and then goes low at 70 units of time; input J is alternately low and high for 10 units of time each (total time duration is 90 units). Draw the output waveform w.r.t. output variable Y for the condition given in the following Verilog statement: assign #5 Y= I^ J;	CO-3	2.5
Q8	Compute the result of the following operations in Verilog HDL: a) Z=p**q for p=5, q=4;	CO-3	1*5=5

	b) out=A>>2 for value of A=4'b0011;
	c) ^A for the value of A= 5'b10010;
	d) Y=(2{P} , 3'b110, 4{Q}) for P=2'b01, Q=1'b1;
	v) Z=!Y for Y=10;		

Q9	What is system on chip (SoC)? Can Field Programmable Gate Arrays (FPGA) serve as a SoC platform? If yes, discuss the key components of FPGA SoC Architecture, its advantages, and key application areas.	CO-3	4