JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATIONS-FEBRUARY 2025

M.Tech-II Semester (ECE)

COURSE CODE (CREDITS): 21M11EC211 (3) MAX. MARKS: 15

COURSE NAME: Digital System Design using Verilog HDL

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 1 Hour

Note: *(a) All questions are compulsory. (b) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems.*

Q. No	Question	CO	Marks
Q1	*Hardware Description Languages (HDLs) offer many advantages over Traditional schematic-based design approaches*, justify this statement with a few technical points.	CO-1	2
Q2	Any digital circuit design can be abstracted in Verilog HDL using various levels of abstraction; discuss with brief description of each of these levels.	CO-1	2.5
Q3	What do instance and instantiation signify in Verilog HDL? Support your answer with a suitable example.	CO-1	2

Q4	Out of the following 2 cases shown, which one is a legal way of doing comments and which one is an illegal way of comments in Verilog HDL. Justify your answer.
	a) /* a=b && c; // d=x^y */
	b) /* z=m? n : p ; /* q=g^h; */ n = ~w */
		CO-2	2

Q5	*Arrays are different from register Vectors*, justify this statement with proper description along with suitable example of each of these.	CO-2	2
Q6	Defparam and localparam are the two important keywords of Verilog HDL. How are these two different from each other?	CO-2	1.5
Q7	Are these legal identifiers in Verilog HDL? a) system1 b) 1reg c) $latch	CO-2	1
Q8	Declare the following variables in Verilog: a) A 32-bit storage register called *address*. Bit 31 must be the MSB. Set the value of the register to a 32-bit decimal number equal to 3. b) An array called delays. Array contains 20 elements of the type integer. c) A memory MEM containing 256 words of 64 bits each.	CO-2	2