JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-3 EXAMINATION-2024

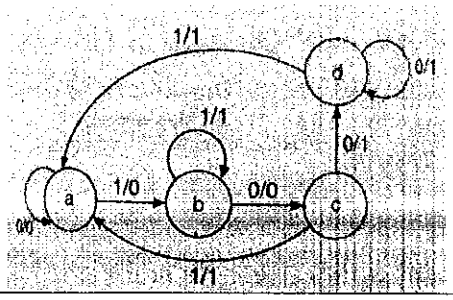
B.Tech-VII Semester (CSE/IT/BT/BI/CE)

COURSE CODE (CREDITS): 20B1WEC734 (3) MAX. MARKS: 35

COURSE NAME: Digital Systems

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 2 Hours

Note: (a) All questions are compulsory. (b) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems.

Q. No	Question	CO	Marks
Q1	A binary ripple counter is required to count up to 4095. How many flip flops are required? If the clock frequency is 9.6 MHZ, what is the frequency at the output of the most significant bit?	CO-3	1.5+1.5=3
Q2	Design a mod-80 ripple counter using cascading.	CO-3	5
Q3	A 4-bits serial-in-serial-out shift register has to be designed using D flip-flops in such a way that the data can be shifted in both (left and right) directions simultaneously on command using the same designed circuit (one circuit only). Draw the logic diagram of such design and explain its working.	CO-2	5
Q4	Design a synchronous decade counter using T flip-flops.	CO-3	5
Q5	Design a sequence detector to detect the binary sequence **1001** using Mealy type finite state machine (FSM) with the help of D flip-flops.	CO-3	7
Q6	Differentiate between Moore and Mealy type finite state machines (FSM).	CO-3	2
Q7	Obtain the state table, reduced state table, reduced state diagram for the state machine whose state diagram is shown in figure. 	CO-4	1+1+1=3

Q8	Draw the algorithmic state machine (ASM) chart for mod-7 synchronous counter.	CO-2	3
Q9	A long sequence of pulses enters a 2-input 2-output synchronous sequential circuit which is required to produce an output z=1, whenever the sequence 1111 occurs. Overlapping sequences are accepted. For example, if the input is 01011111, the required output is 00000011. Draw the state diagram.	CO-3	2