JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2024

B.Tech-V Semester (CSE/IT)

COURSE CODE (CREDITS): 18B11CI514 (3) MAX. MARKS: 35

COURSE NAME: Computer Organization and Architecture

COURSE INSTRUCTORS: Vivek Kumar Sehgal, Vipal Kumar, Praveen Modi, Monika

MAX. TIME: 2 Hours

Note: (a) All questions are compulsory.

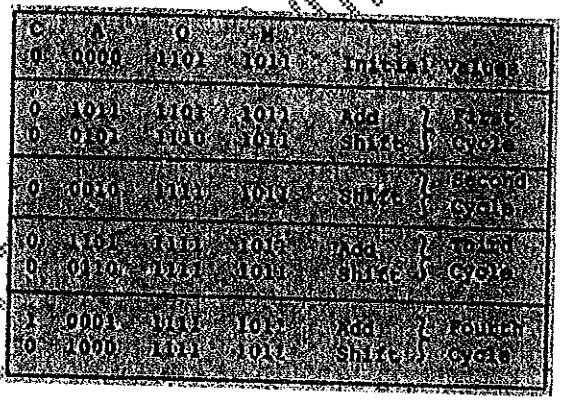
(b) All the parts of a question should be attempted together and in sequence.

Q.No	Question	CO	Marks
Q1	(a) For a pipeline with ' n ' stages, what's the ideal throughput? What prevents us from achieving this ideal throughput?	CO-5	2
	(b) Consider a pipeline having 4 phases with duration 60, 40, 90 and 100 ns. Given latch delay is 10 ns. Calculate- 1. Pipeline cycle time, 2. Non-pipeline execution time, 3. Speed up ratio, 4. Pipeline time for 1000 tasks, 5. Sequential time for 1000 tasks, 6. Throughput		2
	(c) Consider a 4-stage pipeline processor. The number of cycles needed by the four instructions *I1, I2, I3* and *I4* in stages *S1, S2, S3* and *S4* is shown below-		3

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop?
For (i=1 to 2) {I1; I2; I3; I4;}

Q2	(a) What is a pipeline hazard? What are the different types of hazards in a pipelined microprocessor design?	CO-5,6	3
	(b) A non-pipelined instruction execution unit operating at 2 GHz takes an average of 6 cycles to execute an instruction of a program P. The unit is then redesigned to operate on a 5-stage pipeline at 2 GHz. Assume that the ideal throughput of the pipelined unit is 1 instruction per cycle. In the execution of program P, 20% instructions incur an average of 2 cycles stall due to data hazards and 20% instructions incur an average of 3 cycles stall due to control hazards. Calculate the speedup (rounded off to one decimal place) obtained by the pipelined design over the non-pipelined design.		2
	(c) Consider a 3GHz (gigahertz) processor with a three-stage pipeline and stage latencies $\tau_1, \tau_2,$ and τ_3 such that $\tau_1 = 3\tau_2/4 = 2\tau_3$. If the longest pipeline stage is split into two pipeline stages of equal latency,		2

	calculate the new frequency, ignoring delays in the pipeline registers.		
Q3	(a) The value of a float type variable is represented using the single-precision 32-bit floating point format of IEEE−754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A float type variable X is assigned the decimal value of −14.25. What is the representation of X in hexadecimal notation?	CO-3,4	3
	(b) Explain the following three techniques for data transfer: 1) Programmed I/O, 2) Interrupt-driven I/O, 3) Direct memory access		2
	(c) What is the difference between Memory- Mapped and Isolated I/O. Explain with assembly code.		2
Q4	(a) Explain Simple Interrupt Processing triggered through hardware and software	CO-4	2
	(b) Explain three Alternative DMA Configurations		3
	(c) Consider a computer with a 4 MHz processor. Its DMA controller can transfer 8 bytes in 1 cycle from a device to main memory through cycle stealing at regular intervals. Which one of the following is the data transfer rate (in bits per second) of the DMA controller if 1% of the processor cycles are used for DMA?		2
Q5	(a) State the Both's algorithm for multiplication of two numbers, Draw a block diagram for the implementation of the Booth's algorithm for determining the product of two 8-bit signed numbers	CO-6	3
	(b) Give the Hardware Implementation of Unsigned Binary Multiplication. 		2
	(c) A device with data transfer rate *10 KB/sec* is connected to a *CPU*. Data is transferred byte-wise. Let the interrupt overhead be *4 µsec*. The byte transfer time between the device interface register and *CPU* or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode?		2