JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-2 EXAMINATION-OCTOBER-2024

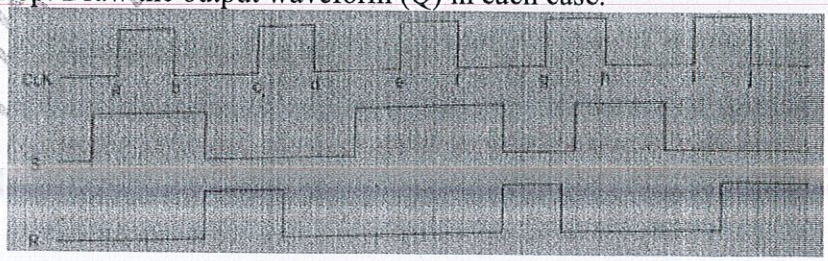
B.Tech-VII Semester (CSE/IT/BT/BI/CE)

COURSE CODE (CREDITS): 20B1WEC734 (3) MAX. MARKS: 25

COURSE NAME: Digital Systems

COURSE INSTRUCTOR: Dr. Pardeep Garg MAX. TIME: 1.5 Hours

Note: (a) All questions are compulsory. (b) Marks are indicated against each question in square brackets. (c) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems.

Q. No	Question	CO	Marks
Q1	Design a full adder using 1:8 demultiplexer.	CO-1,3	2
Q2	Design 2-input AND, NOR, and XOR gate using suitable multiplexer (show output for each case separately).	CO-1,3	2
Q3	Employing the logic diagram of 4-bit binary parallel adder-subtractor (using full-adders in one circuit), explain its working.	CO-1,3	3
Q4	A priority encoder with 4 decimal inputs (A {MSD}, B, C, and D {LSD}) where A is having the lowest priority and D is having the highest priority has to be designed. Obtain the truth table for it.	CO-1,3	2
Q5	A combinational circuit having four inputs and one output has to be designed in such a way that the output is equal to 1 when (a) all the inputs are equal to 1, (b) none of the inputs are equal to 1, (c) an odd number of inputs are equal to 1. i) Obtain the truth-table for it. ii) Design it using 8:1 multiplexer.	CO-1,3	3
Q6	Design a 32:1 multiplexer using 8:1 multiplexers (all having active-high enable input) & 2:4 decoder (all in one-circuit only).	CO-1,3	3
Q7	The waveforms shown in the figure are applied to (a) a positive-edge triggered S-R flip-flop, (b) a negative-edge triggered S-R flip-flop. Draw the output waveform (Q) in each case. 	CO-2	3
Q8	Why does race-around condition occur? How can it be solved using Master-Slave flip-flop design? Discuss both in detail.	CO-2	1.5+2.5=4
Q9	Design a logic circuit which converts D flip-flop to J-K flip-flop.	CO-2	3