JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- 2024

B.Tech-V Semester (CSE/IT)

COURSE CODE (CREDITS): 18B11CI514 (3) MAX. MARKS: 25

COURSE NAME: Computer Organization and Architecture

COURSE INSTRUCTORS: Vivek Kumar Sehgal, Vipal Kumar, Praveen Modi, Monika

MAX. TIME: 1 Hour 30 Minutes

Note: *(a) All questions are compulsory.*

(b) All the parts of a question should be attempted together and in sequence.

Q.No	Question	CO	Marks
Q1	(a) What you mean by the memory hierarchy? Explain it by a memory pyramid	CO-2,3	2
	(b) Name the different cache mapping techniques		1
	(c) Consider a direct mapped cache of size 32KB with block size 32 bytes. The CPU generates 32 bit addresses. Calculate the number of bits needed for cache indexing and the number of tag bits.		2
Q2	(a) What are the advantages and disadvantages of direct mapping?	CO-3	2
	(b) A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. Calculate the number of bits for the TAG field.		2
	(c) What do you mean by locality of reference in cache memory?		1
Q3	(a) Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. Calculate the number of cache misses for the following sequence of block addresses is: 8,12,0,12,8.	CO-3	1
	(b) Consider a fully associative cache with 8 cache blocks (numbered 0-7) and the following sequence of memory block requests : 4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7. If LRU replacement policy is used, which cache block will have memory block 7?		2
	(c) Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks are in the following order: 0,255,1,4,3,8,133,159,216,129,63,8,48,32,73,92,155. Which one of the memory block/set will NOT be in cache if LRU replacement policy is used?		2
Q4	(a)The access time of cache memory is 45 *nsec* and that of main memory is 750 *nsec*. It is found that 75% of memory requests are for		1

	read and remaining for write. If the hit access for read is 0.9 and hit ratio for write is 1 and write through protocol is used, then calculate the average memory access time.		
	(b) A cache memory that has a hit rate of 0.8 has an access latency 10ns and miss penalty 100ns. An optimization is done on the cache to reduce the miss rate. However, the optimization results in an increase of cache access latency to 15ns, whereas the miss penalty is not affected. What is the minimum hit rate (rounded off to two decimal places) needed after the optimization such that it should not increase the average memory access time?	CO-3,4	2
	(c) In a two-level cache system, the access times of L1 and L2 caches are 1 and 8 clock cycles, respectively. The miss penalty from the L2 cache to main memory is 18 clock cycles. The miss rate of L1 cache is twice that of L2. The average memory access time (AMAT) of this cache system is 2 cycles. Calculate the miss rates of L1 and L2 respectively.		1
	(d) The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. Calculate the average memory access time (in nanoseconds) in executing the sequence of instructions.		2
Q5	(a) Draw the typical memory cell structures for: a. Dynamic RAM (DRAM) cell b. Static RAM (SRAM) cell	CO-4	2
	(b) What is RAID? Give a small description of different Seven (0-6) RAID Levels.		2