JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- 2024

MSc -3rd Semester (Physics)

COURSE CODE (CREDITS): 24MS3PH301 (3) MAX. MARKS: 25

COURSE NAME: Electronics-II

COURSE INSTRUCTORS: SKK MAX. TIME: 1 Hour 30 Minutes

Note: *(a) All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

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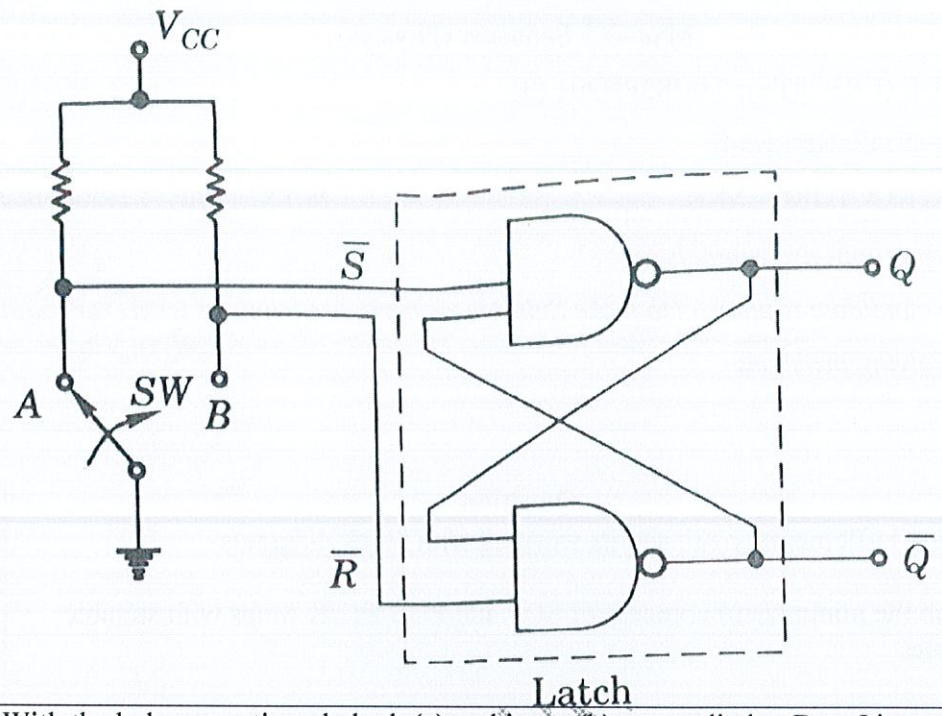
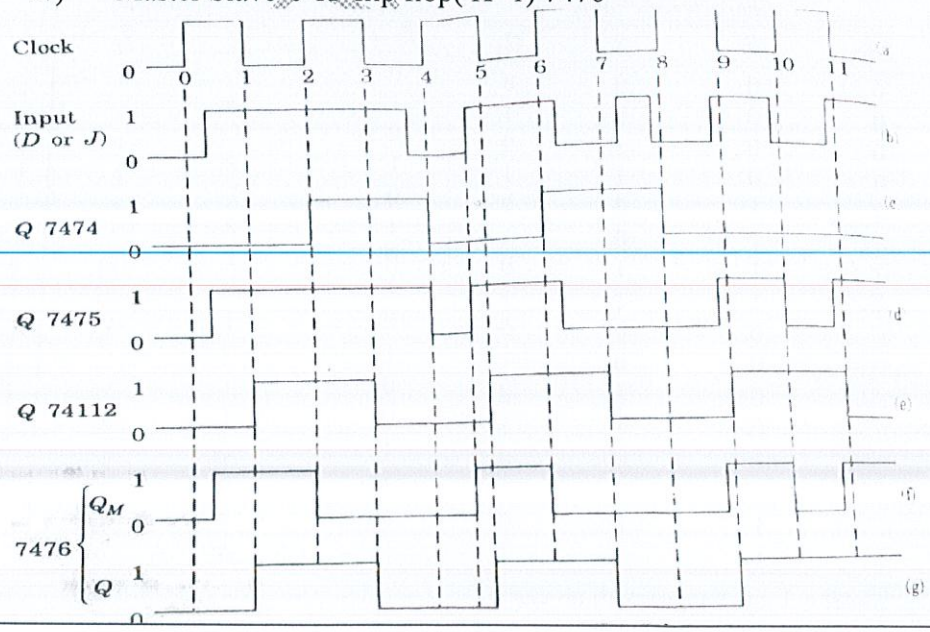
Q.No	Question	Marks
1	Define a 1-Bit memory cell and its working with block diagrams	3
2	Explain the minimization process of SOP and POS 2x2 K Maps with suitable examples	5
3	Differentiate between D-Type and T-Type flip-flop s with block diagrams and truth tables	4
4	Design a R-S flip flop with the following characteristic table	4

Characteristic table | *Truth table for decoder*

CK	S	R	Q_n	Q_{n+1}	Y_1	Y_2	
0	0	0	0	0	1	×	
0	0	0	1	1	×	1	
0	0	1	0	0	1	×	
0	0	1	1	1	×	1	
0	1	0	0	0	1	×	
0	1	0	1	1	×	1	
0	1	1	0	0	1	×	*
0	1	1	1	1	×	1	*
1	0	0	0	0	1	×	
1	0	0	1	1	×	1	
1	0	1	0	0	1	×	
1	0	1	1	0	1	0	
1	1	0	0	1	0	1	
1	1	0	1	1	×	1	
1	1	1	0	×	×	×	**
1	1	1	1	×	×	×	**

*$S = R = 1$ can happen with no clock.

**$S = R = 1$ must not happen.

5	Show that the circuit acts as bounce elimination switch  	4
6	With the below mentioned clock (a) and input (b) are applied to D or J input of each of the following flip-flops, sketch the output wave form of the following i) Positive edge triggered D type flip flop 7474 ii) Positive level triggered D type flip flop 7475 iii) Negative edge triggered J-K flip flop(K=1) 74112 iv) Master Slave J-K flip flop(K=1) 7476  	5