JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- 2024

MSc-III Semester (Physics)

COURSE CODE(CREDITS): 24MS3PH301(3) MAX. MARKS: 15

COURSE NAME: Electronics II

COURSE INSTRUCTORS: SKK MAX. TIME: 1 Hour

Note: (a)*All questions are compulsory.*

(b)Marks are indicated against each question in square brackets.

1. Given the Logical Equation $Y = (A + BC)(B + \bar{C}\,A)$
   (a) Design circuit using basic logic gates.
   (b) Is it possible to design circuit using NAND gate, If yes design the circuit.
   (c) Simplify the equation.
   (d) If the design is simplified, Design the circuit using NOR gates.
   (e) Compare the three circuits in terms of no of inputs, no of gates and type of gates.

(1x5)

2. Minimize the four variable logic function using K-maps
   (a) $f(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,11,14) using\ SOP$
   (b) $f(A,B,C,D) = \prod M(4,6,10,12,13,15) using\ POS$
   (c) $f(A,B,C,D) = \sum m(0,3,5,6,9,10,12,15) using\ SOP$

(1+1+1)

3. Implement the following multi output combinational logic circuit using a 4 to 16 line decoder

   $F1 = \sum m(1,2,4,7,8,11,12,13)$ $F2 = \sum m(2,3,9,11)$ $F3 = \sum m(10,12,13,14)$ $F4 = \sum m(2,4,8)$

(2.5)

4. Carry is always there in full adder and half adder, How are they different in operations

(2)

5. Design a 4 input logic circuit, having output as 1 only when any two inputs are 1. For all other conditions the output is 0

(2.5)