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ZIGBEE BASED WIRELESS ELECTRONIC NOTICE BOARD

Project Report submitted in partial fulfillment of the requirement for the degree of

Bachelor of Technology

in

Electronics and Communication Engineering

under the Supervision of

Dr. Neeru Sharma

By

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Certificate

This is to certify that project report entitled "**Zigbee based wireless electronic notice board**", submitted by **Palak Dewan(091019), Sonali Magotra(091071), Aditi Sharma(091094)** in partial fulfillment for the award of degree of Bachelor of Technology in Electronics and Communication Engineering to Jaypee University of Information Technology, Waknaghat, Solan has been carried out under my supervision.

This work has not been submitted partially or fully to any other University or Institute for the award of this or any other degree or diploma.

Date: 28.5.13

NS Sharma

Dr. Neeru Sharma

Assistant Professor

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Date: 28·5·13

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ABSTRACT

This project deals about designing a wireless notice board which can be accessed remotely using advanced Zigbee technology. Zigbee is a PAN technology based on the IEEE 802.15.4 standard. This technology is a low data rate, low power consumption, low cost, wireless networking protocol targeted towards automation and remote control applications. In terms of battery life, cost, complexity of protocol stack and number of nodes participating in mesh network zigbee is better than other WPANs, such as Bluetooth. It is one of the new technology in the embedded field to make the communication between microcontroller and computer. ZigBee uses a basic master-slave configuration suited to static star networks of many infrequently used devices that talk via small data packets. The hardware of the project consists of two parts: Zigbee transmitting module and Zigbee receiving module. The keyboard is connected on the transmitter side, whatever the text is typed on the transmitter side the same is the received on the receiver side. Messages can be transmitted to multi-point receivers. After entering the text, the user can disconnect the keyboard. At any time the user can add or remove or alter the text according to his requirement. The project is built around the AT89C51 micro controller from Atmel. This micro controller provides all the functionality of the display and wireless control. Assembly language is used to program the microcontroller.

CHAPTER 1

INTRODUCTION

1.1 Objective of the project

Notice Board is primary thing in any institution / organization or public utility places like bus stations, railway stations and parks. But sticking various notices day-to-day is a difficult process. A separate person is required to take care of this notices display.also the alteration in notices require a new hard copy.Mostly all electronic notice boards are designed using wired system.One of the drawbacks of the design is the inflexibility in terms of placement.the common notice board cannot be placed anywhere because of the messy wire.So our proposed idea i.e wireless electronic notice board has replaced the system of wires.It is used as user friendly notice board with wireless concept that allows user to control the information display between 75-100m range. This high-tech technology overcomes previous issues and eliminates manual work upto some extent.

1.2 Zigbee technology

ZigBee technology is a low data rate, low power consumption, low cost, wireless networking protocol targeted towards automation and remote control applications.Zigbee has a defined rate of 250 kbit/s, best suited for periodic or intermittent data or a single signal transmission from a sensor or input device. The technology defined by the ZigBee specification is intended to be simpler and less expensive than other WPANs, such as Bluetooth. It requires only about 10% of the software of a typical Bluetooth. ZigBee devices have the ability to form a mesh network between nodes. Meshing is a type of daisy chaining from one device to another. This technique allows the short range of an individual node to be expanded and multiplied, covering a much larger area.

IEEE 802.15.4 committee started working on a low data rate standard a short while later. Then the ZigBee Alliance and the IEEE decided to join forces and ZigBee is the

commercial name for this technology.IEEE 802.15.4 is now detailing the specification of PHY and MAC by offering building blocks for different types of networking known as "star, mesh, and cluster tree". Network routing schemes are designed to ensure power conservation, and low latency through guaranteed time slots. A unique feature of ZigBee network layer is communication redundancy eliminating single point of failure in mesh networks. Key features of PHY include energy and link quality detection, clear channel assessment for improved coexistence with other wireless networks.

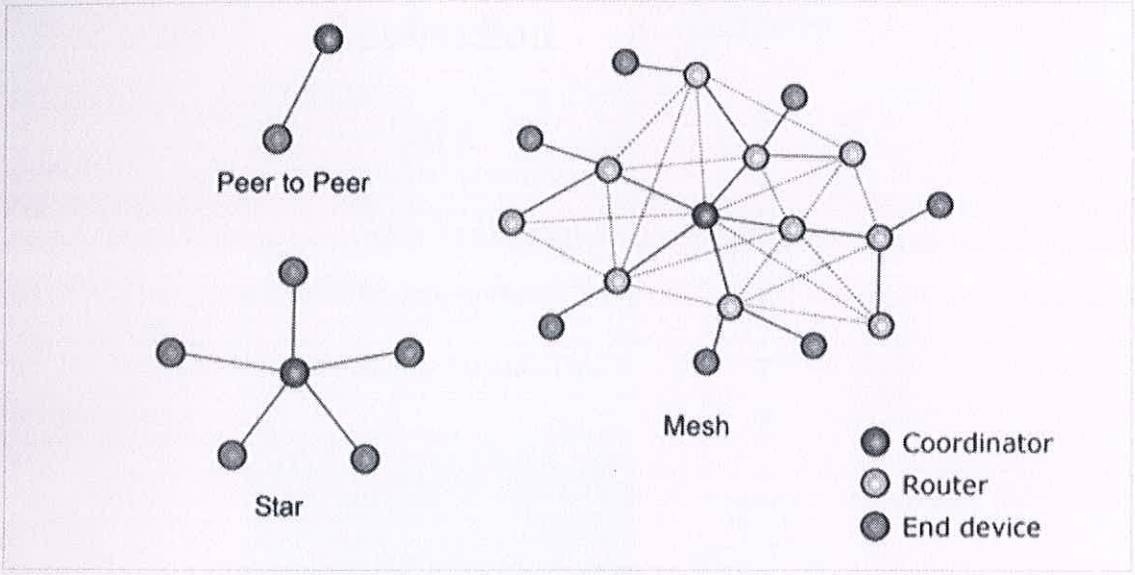


Figure 1: Types of topologies

The PHY provides two services : the PHY data service and PHY management service interfacing to the physical layer management entity (PLME). The PHY data service enables the transmission and reception of PHY protocol data units (PPDU) across the physical radio channel.The features of the PHY are activation and deactivation of the radio transceiver, energy detection (ED), link quality indication (LQI), channel selection, clear channel assessment (CCA) and transmitting as well as receiving packets across the physical medium.

The MAC sublayer provides two services: the MAC data service and the MAC management service interfacing to the MAC sublayer management entity (MLME)

service access point (SAP) (MLMESAP). The MAC data service enables the transmission and reception of MAC protocol data units (MPDU) across the PHY data service. The features of MAC sublayer are beacon management, channel access, GTS management, frame validation, acknowledged frame delivery, association and disassociation

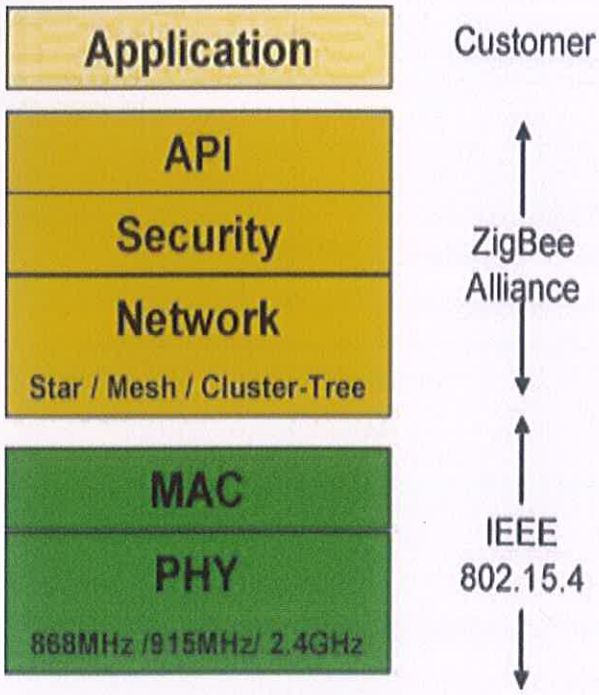


Figure 2: Protocol stack of Zigbee

1.3 Comparison of other technologies

FEATURE(S)	IEEE 802.11	BLUETOOTH	ZIGBEE
Battery life	Hours	Days	Years
Complexity	Very complex	Complex	Simple
Nodes	32	7	64000
Latency	up to 3seconds	10 seconds	30 milliseconds
Range	100m-1000m	10m	10-75m
Data rate	11Mbps	1Mbps	250Kbps

Table 1: Comparison of other technologies

1.4 Organisation of the report

This report has been divided into various chapters . Brief description of these chapters is given below

Chapter1: It gives an overview of the project as well as the objective of the project

Chapter2: It covers the basic circuit diagram of the Transmitter and Receiver, simulation of the circuits and the brief description of the software used for coding the microcontroller.

Chapter3: It reviews the hardware description of each circuitry and the list of component used in this project.

CHAPTER 2

CIRCUIT SIMULATION

2.1 Circuit Diagram

The entire project has been divided into two parts:

- Transmitter
- Receiver

2.1.1 Circuit Diagram of Transmitter

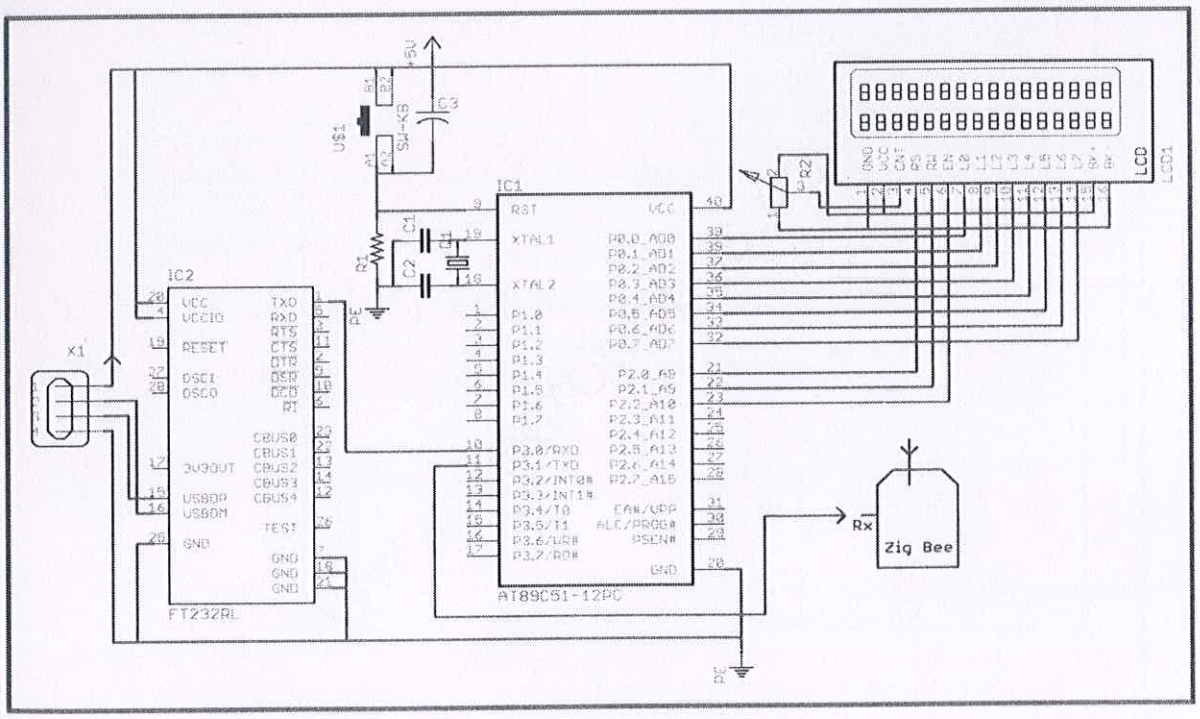


Figure 3:Circuit diagram of Transmitter

Microcontroller has four 8-bit ports .Pin 40 of the microcontroller is set at Vcc= +5V.Pin 20 is grounded .A 12 Mhz crystal oscillator is connected between pin 18 and 19.A 16X2 lcd is interfaced at the output side of the microcontroller .8 bit data pins of the lcd from DB0 to DB7 are connected at port 0 of microcontroller(P0.0 to P0.7).Data pin8 (DB7) of the LCD is busy flag and is read when R/W = 1 & RS = 0. When busy flag=1, it means that LCD is not ready to accept data since it is busy with the internal operations. Therefore before passing any data to LCD, its command register should be read and busy flag should be checked.

2.1.2 Circuit Diagram Of Receiver

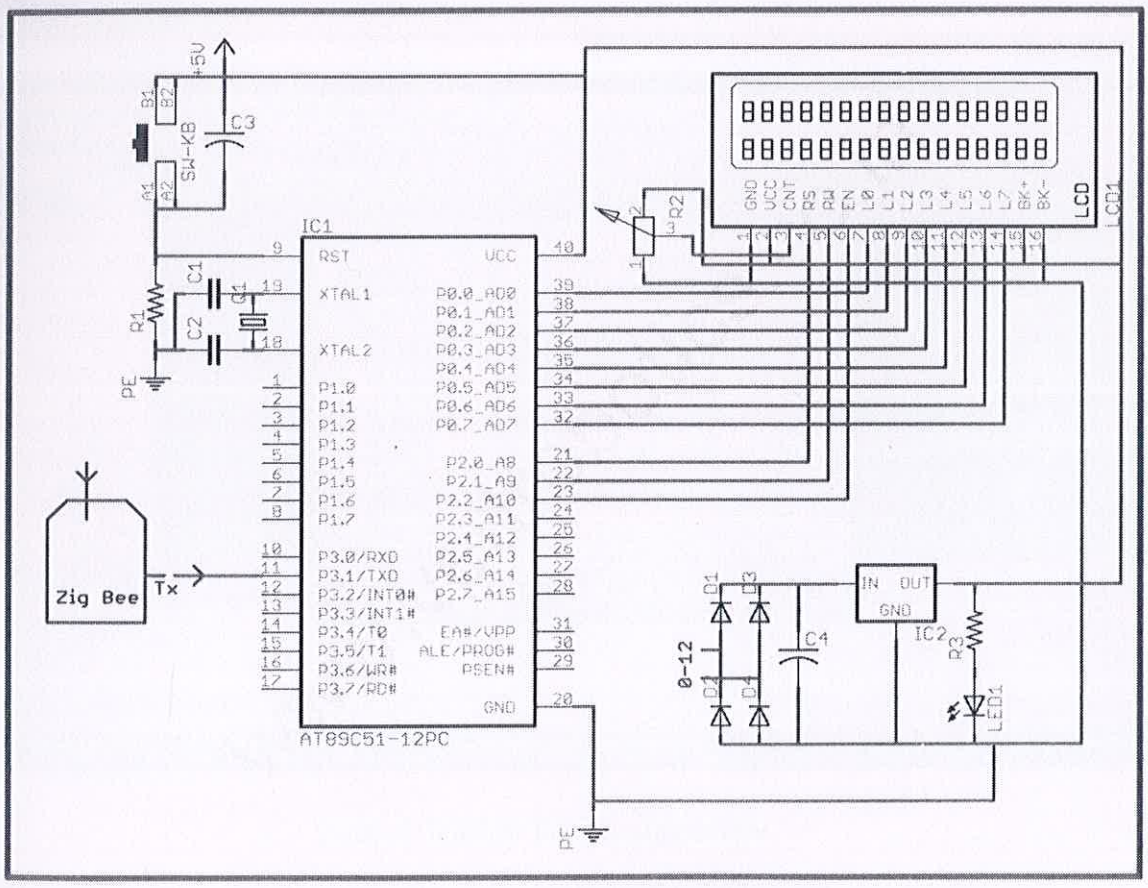


Figure 4:Circuit diagram of Receiver

To send data on the lcd, data is first written to data pins with R/W = 0(to specify the write operation) and RS = 1(to select data register).A high to low pulse is given at EN pin when data is sent .To send a command on the lcd, the command is first specified to data pins with R/W=0 and R/S =0 (to select the command register).

2.2 Coding

2.2.1 Keil Software

KEIL uVision is the name of the software dedicated to the development and testing of a family of microcontroller based on 8051 technology , like the 89S52 which we are going to use along this project.

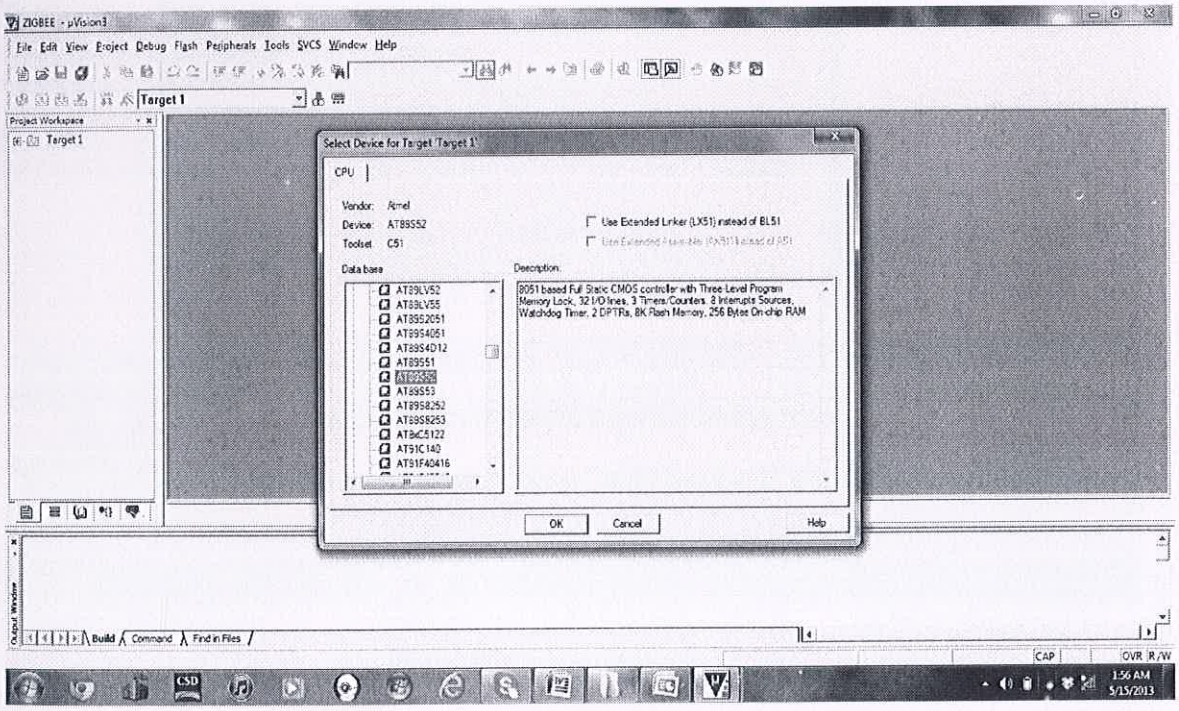


Figure 5:Window for selecting device

2.2.2 Creating Hex File

Any communication with the microcontroller is done in the hex code .So,the programming which is done in the assembly language is first to be converted into hex code . KEIL uVision software was used to generate the HEX code that will be transferred to the microcontroller. The code is written in the target window and command is given for creating the hex file .As a result, the desired hex file is made which is saved in the same location as the project folder.

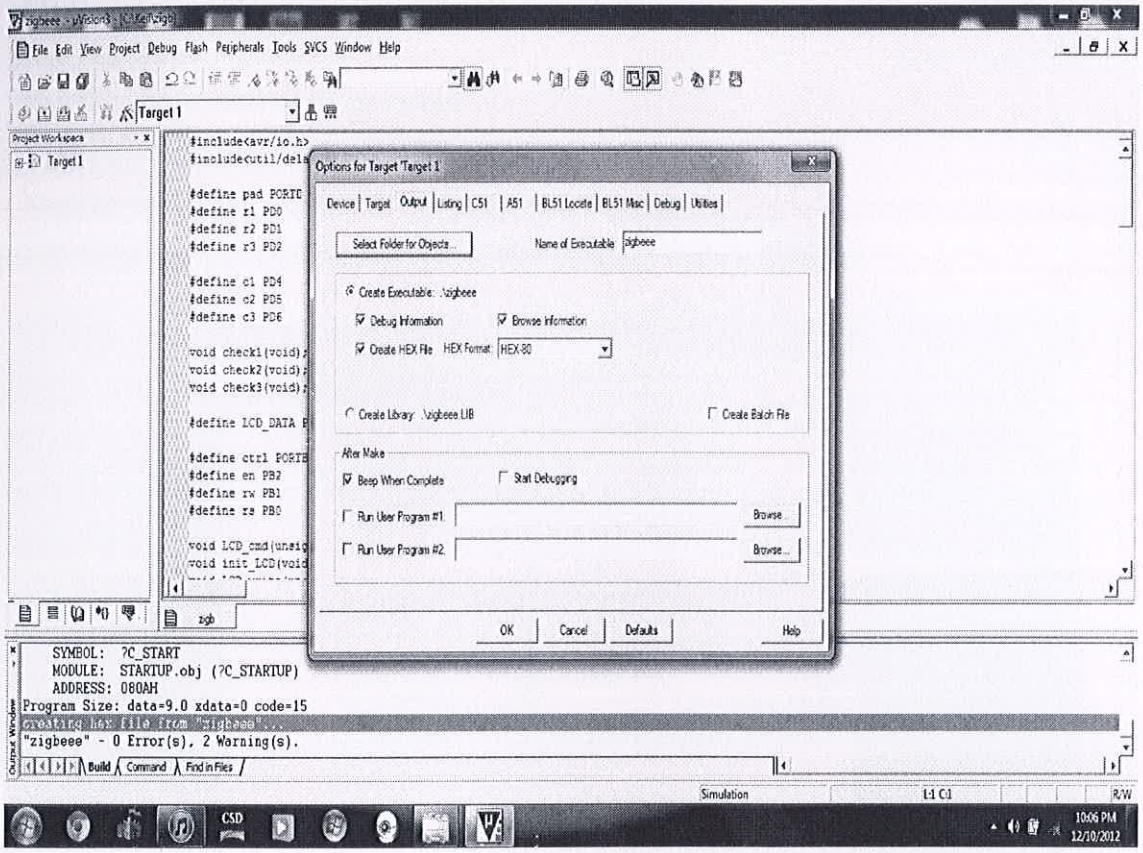


Figure 6: Creating hex file

2.2.3 Flash Magic

Flash Magic is Windows software from the Embedded Systems Academy that allows easy access to all the ISP features provided by the devices. These features include:

· Erasing the Flash memory (individual blocks or the whole device)

· Programming the Flash memory

· Modifying the Boot Vector and Status Byte

· Reading Flash memory

· Performing a blank check on a section of Flash memory

· Reading the signature bytes

· Reading and writing the security bits

· Direct load of a new baud rate (high speed communications)

· Sending commands to place device in Bootloader mode

Flash Magic provides a clear and simple user interface to these features

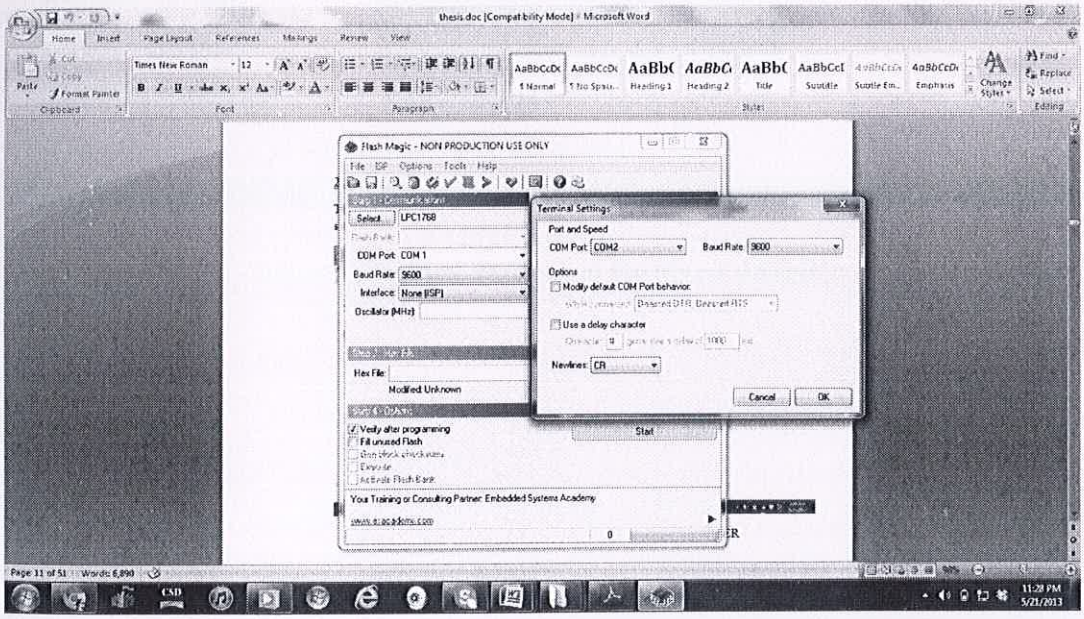


Figure 7: Flash Magic

2.2.4 Programming the Microcontroller

Flash Magic software is used to transfer the program to the microcontroller. The microcontroller is attached to the system then the the HEX file is loaded in the software which is then burnt to the microcontroller .In this way the desired code is written in the microcontroller. Now, the microcontroller is ready to be used in the circuit.

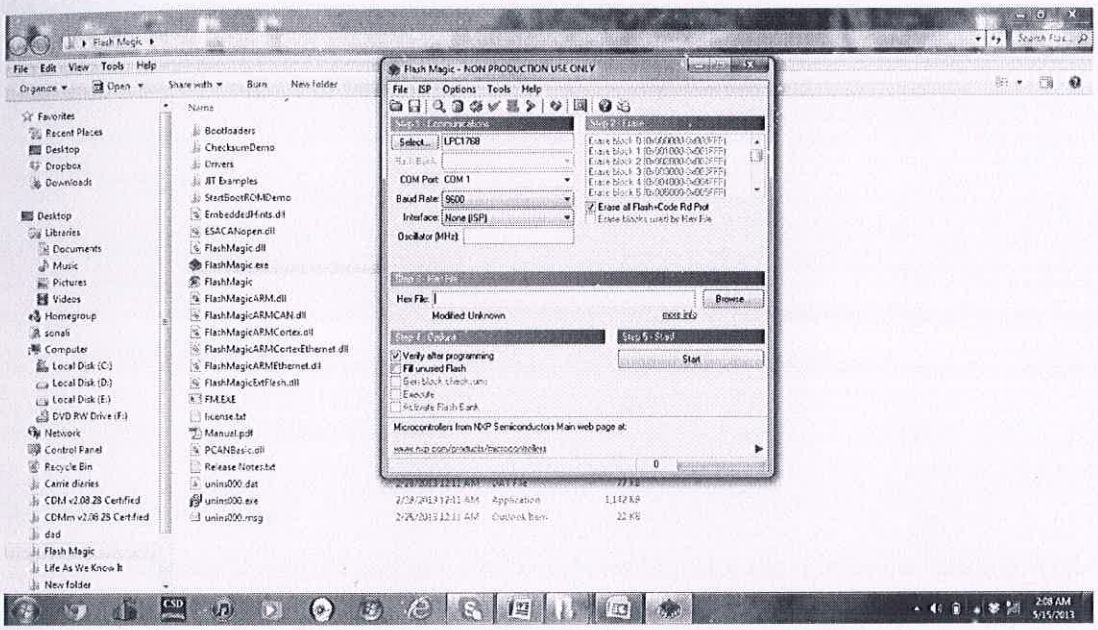


Figure 8: Burning the code to the microcontroller

CHAPTER 3

HARDWARE DESIGN

The hardware setup consists of the following major components

1. AT89S51 Microcontroller
2. 16*2 LCD
3. IC 7805
4. Zigbee transceiver
5. FT232RL
6. Power Supply

3.1 Microcontroller

A microcontroller is a small and low cost computer built for the purpose of dealing with specific tasks, such as displaying information on led, receiving information from the zigbee module or receiving information from television's remote control. Microcontrollers are mainly used in products that require a degree of control to be exerted by the user. A microcontroller is a small computer on a single integrated circuit containing a processor core, memory, and programmable input/output peripherals. Program memory in the form of NOR flash or OTP ROM is also often included on chip, as well as a typically small amount of RAM. Microcontrollers are designed for embedded applications, in contrast to the microprocessors used in personal computers or other general purpose applications. Microcontrollers are used in automatically controlled products and devices, such as automobile engine control systems, implantable medical devices, remote controls, office machines, appliances, power tools, toys and other embedded systems.

Microcontrollers usually contain from several to dozens of general purpose input/ output pins(GPIO). GPIO are software configurable to either an input or output stage. When GPIO pins are configured to input state, they are often used to read sensors or external signals. Configured to the output stage GPIO pins can drive external devices such as LED, LCD or motors.

ATMEL AT89 Series

The Atmel AT89 series is an Intel 8051-compatible family of 8 bit microcontrollers (μCs) manufactured by the Atmel Corporation. Based on the Intel 8051 core, the AT89 series remains very popular as general purpose microcontrollers, due to their industry standard instruction set, and low unit cost. This allows a great amount of legacy code to be reused without modification in new applications. While considerably less powerful than the newer AT90 series of AVR RISC microcontrollers, new product development has continued with the AT89 series for the aforementioned advantages.

AT89 Series Microcontrollers

Device name		Data Memory
AT89C1051	1K Flash	64 RAM
AT89C2051	2K Flash	128 RAM
AT89C4051	4K Flash	128 RAM
AT89C51	4K Flash	128 RAM
AT89C52	8K Flash	256 RAM
AT89C55	20K Flash	256 RAM
AT89S8252	8K Flash	256 RAM
AT89S53	12K Flash	256 RAM

Port Structures and Operation

All four ports in the AT89C51 and AT89C52 are bidirectional. Each consists of a latch (Special Function Registers P0 through P3), an output driver, and an input buffer. The output drivers of Ports 0 and 2, and the input buffers of Port 0, are used in accesses to external memory. In this

application, Port 0 outputs the low byte of the external memory address, time-multiplexed with the byte being written or read. Port 2 outputs the high byte of the external memory address when the address is 16 bits wide. Otherwise the Port 2 pins continue to emit the P2 SFR content. All the Port 3 pins, and two Port 1 pins (in the AT89C52) are multifunctional. They are not only port pins, but also provide the special features listed in the following table.

Port Pin	**Alternate Function**
P1.0	T2 (Timer/Counter 2 external input)
P1.1	T2EX (Timer/Counter 2 Capture/Reload trigger)
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt)
P3.3	INT1 (external interrupt)
P3.4	T0 (Timer/Counter 0 external input)
P3.5	T1 (Timer/Counter 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Table 2: Port pin specification

The 8051 microcontroller architecture

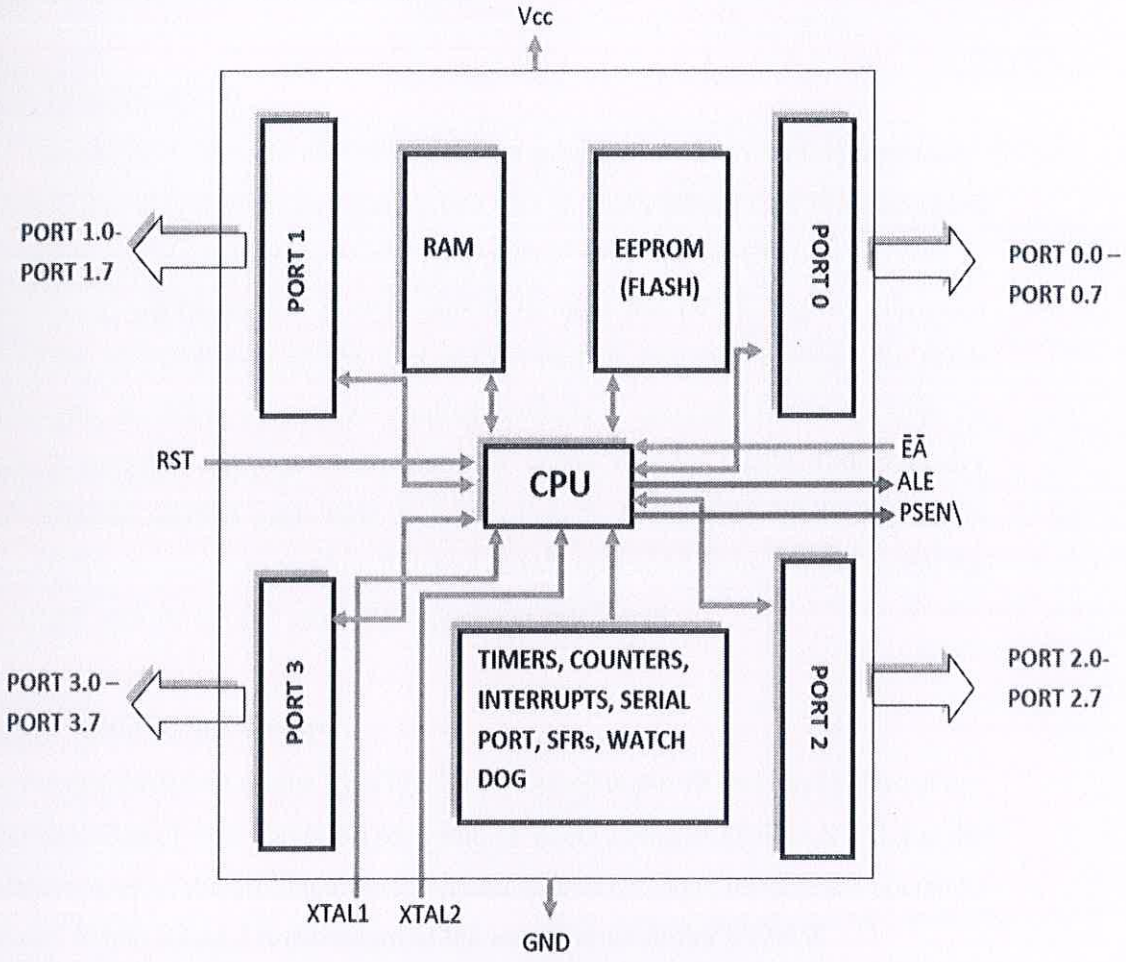


Figure 9: 8051 microcontroller architecture

Figure shows the main features and components that the designer can interact with. You can notice that the 89S51 has four different ports, each one having eight input/output lines providing a total of 32 I/O lines. Those ports can be used to output data and other necessary information i.e. read and write to the LCD.

Most of the ports of 89S51 have dual function that means they can be used for two different functions- one is to perform I/O operations and second is to implement special features of the microcontroller like counting external pulses, interrupting the execution of

the program according to external events, performing serial data transfer or connecting the chip to the computer to update the software.

Memory Organization

All 8051 devices have separate address spaces for program memory and data memory. The logical separation of program memory and data memory allows data to be accessed by 8 bits which can be quickly stored and manipulated with an 8 bit CPU. In addition 16 bit data memory addresses can also be raised through the DPTR register. Program memory(ROM, EPROM) can only be read and not written. Program memory can reach up to 64K bytes. At 89S51 4K bytes of program memory is contained within the chip. To read external program memory microcontroller sends a signal PSEN. Data memory occupies a separate address space from program memory. In the 8051 family, the lowest 128 bytes of data memory are on chip. External RAM(up to 64K bytes). In accessing the external RAM, microcontroller sends RD signal and WR signal.

Oscillator and clock concept

Provided on-chip oscillator driven by XTAL is connected to pin 18 and pin 19. Necessary stabilizing capacitor of 30pf. Great XTAL value of about 3Mhz to 33Mhz. XTAL1 is the input to the reversal of the oscillator amplifier and an internal clock input to the operation of the circuit. While XTAL2 is the output of the oscillator amplifier reversal.

The clock concept is found in all modern digital electronics, it's a simple circuit that will generate pulses of electricity at a very specific frequency. These pulses will cadence all the events happening inside a microcontroller, and will assure the synchronization of the events between various components inside the microcontroller.

AT89S51

The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of In-System Programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM con-tents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset. Some of the features are Compatible with MCS®-51 Products, 4K Bytes of In-System Programmable (ISP) Flash Memory – Endurance: 10,000 Write/Erase Cycles , 4.0V to 5.5V Operating Range, Fully Static Operation: 0 Hz to 33 MHz, Three-level Program Memory Lock, 128 x 8-bit Internal RAM, 32 Programmable I/O Lines, Two 16-bit Timer/Counters, Six Interrupt Sources, Full Duplex UART Serial Channel, Low-power Idle and Power-down Modes, Interrupt Recovery from Power-down Mode, Watchdog Timer, Dual Data Pointer, Power-off Flag, Fast Programming Time.

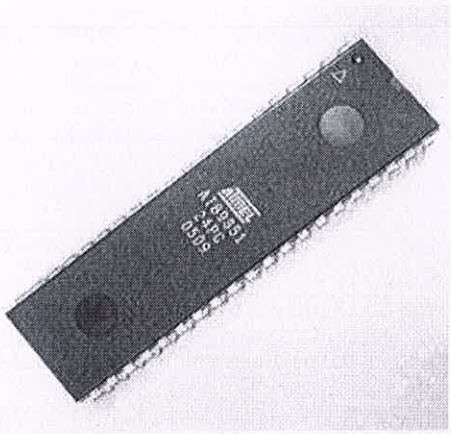


Figure 10:AT89S51 Microcontroller

Pin Description

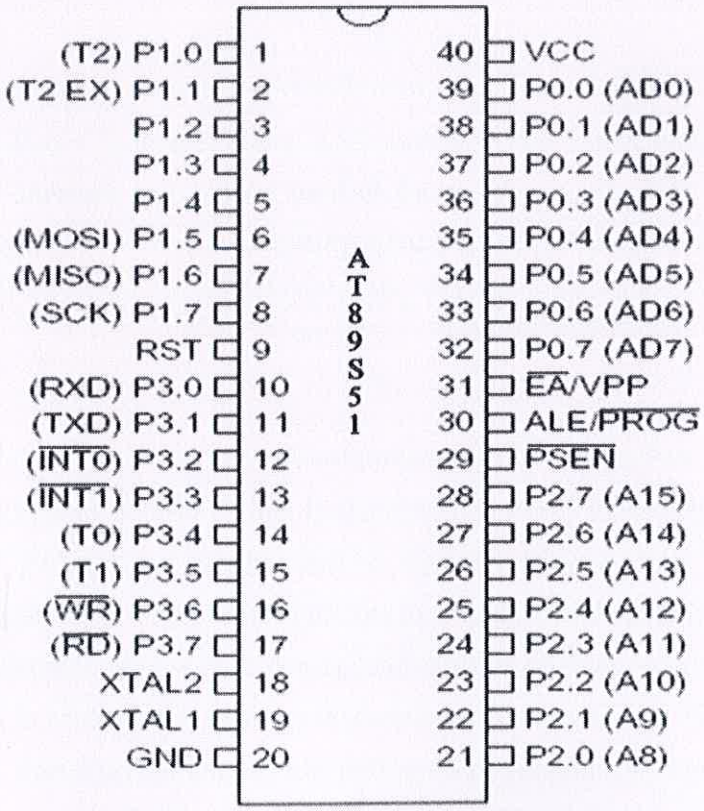


Figure 11: Pin diagram of AT89S51

VCC -Supply voltage

GND -Ground.

Port 0 –

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs. Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups. Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. External pull-ups are required during program verification.

Port 1 –

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2 –

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL) because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the high-order address bits and

some control signals during Flash programming and verification.

Port 3 –

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL) because of the pull-ups. Port 3 receives some control signals for Flash programming and verification. Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	WR (external data memory write strobe)
P3.7	RD (external data memory read strobe)

Table 3:Functioning of port 3 pins

RST -

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DIS-RTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

ALE/PROG –

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input (PROG) during Flash programming. In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory. If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN –

Program Store Enable (PSEN) is the read strobe to external program memory. When the AT89S51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to exter-nal data memory.

EA/VPP –

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset. EA should be strapped to VCC for internal program executions. This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming.

XTAL1 -Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2- Output from the inverting oscillator amplifier

Registers and Memory

Special Function Register - A map of the on-chip memory area called the Special Function Register (SFR) space. Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect. User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

Interrupt Registers - The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

Dual Data Pointer Registers - To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H- 83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should ALWAYS initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

Power Off Flag - The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to "1" during power up. It can be set and rest under software control and is not affected by reset.

Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

Program Memory

If the EA pin is connected to GND, all program fetches are directed to external memory. On the AT89S51, if EA is connected to VCC, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

Data Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT over-flows, it will drive an output RESET HIGH pulse at the RST pin.

Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only

register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode. To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode. Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode. With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51.

Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. Counting binary for Timer 0 TL0 register is formed by (Timer 0 Low Byte, memory-internal data 6AH number) and register TH0 (Timer 0 High Byte, memory-internal data 6CH numbers).Counting binary for Timer 1 registers formed with TL1 (Timer 1 Low Byte, memory-internal data 6BH number) and register TH1 (Timer 1 High Byte, memory-internal data 6DH numbers). To regulate Timer / Counter used two additional registers that are shared by Timer 0 and Timer 1. Additional registers are registers TCON (Timer Control Register, the number of internal data memory-88H, the address can be a bit) and register TMOD (Timer Mode Register, the number of internal data memory-89H).

Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts (INT0 and INT1), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in table given below. Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once. Note that Table shows that bit positions IE.6 and IE.5 are unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products. The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

Symbol	Position	Function
EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
-	IE.6	Reserved
-	IE.5	Reserved
ES	IE.4	Serial Port interrupt enable bit
ET1	IE.3	Timer 1 interrupt enable bit
EX1	IE.2	External interrupt 1 enable bit
ET0	IE.1	Timer 0 interrupt enable bit
EX0	IE.0	External interrupt 0 enable bit

Table 4:Functions of interrupts

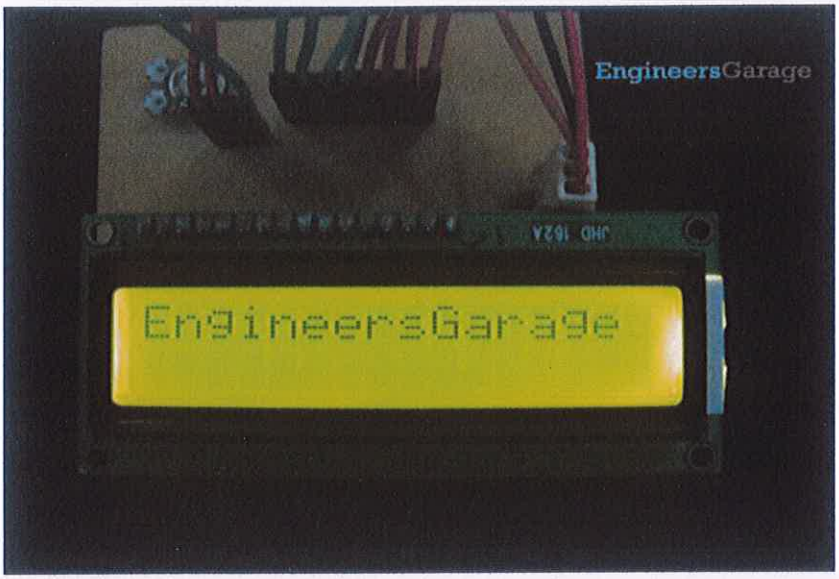
User software should never write 1s to reserved bits, because they may be used in future AT89 products.

3.2 16*2 LCD

LCD (Liquid Crystal Display) screen is an electronic display module and find a wide range of applications. A 16x2 LCD display is very basic module and is very commonly used in various devices and circuits. These modules are preferred over seven segments and other multi segment LEDs. The reasons being: LCDs are economical; easily programmable; have no limitation of displaying special & even custom characters (unlike in seven segments), animations and so on.

A **16x2 LCD** means it can display 16 characters per line and there are 2 such lines. In this LCD each character is displayed in 5x7 pixel matrix. This LCD has two registers, namely, Command and Data.The command register stores the command instructions

given to the LCD. A command is an instruction given to LCD to do a predefined task like initializing it, clearing its screen, setting the cursor position, controlling display etc. The data register stores the data to be displayed on the LCD. The data is the ASCII value of the character to be displayed on the LCD.



Pin description

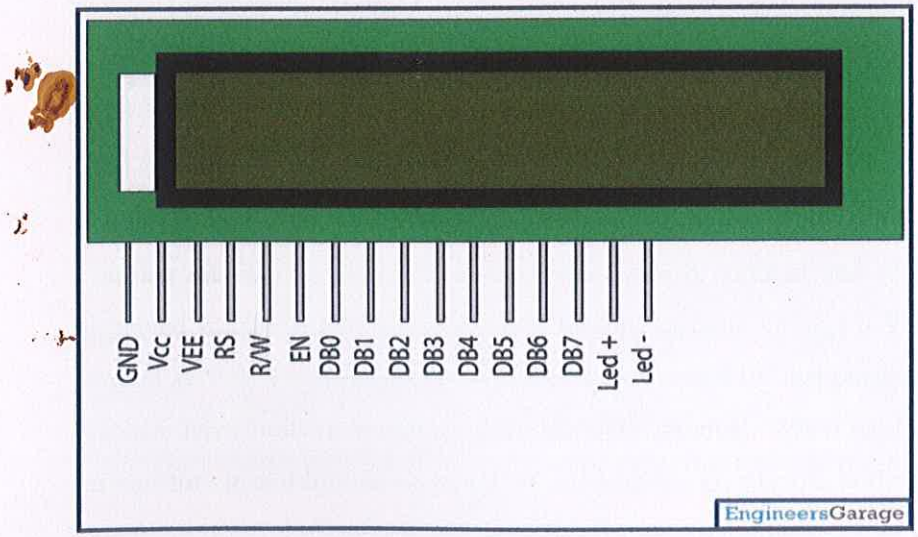


Figure 12: LCD Pin diagram

Pin No	Function	Name
1	Ground (0V)	Ground
2	Supply voltage; 5V (4.7V – 5.3V)	Vcc
3	Contrast adjustment; through a variable resistor	V_{EE}
4	Selects command register when low; and data register when high	Register Select
5	Low to write to the register; High to read from the register	Read/write
6	Sends data to data pins when a high to low pulse is given	Enable
7	8-bit data pins	DB0
8		DB1
9		DB2
10		DB3
11		DB4
12		DB5
13		DB6
14		DB7
15	Backlight V_{CC} (5V)	Led+
16	Backlight Ground (0V)	Led-

Table 5: LCD pin functions

Contrast on display depends on the power supply voltage and whether messages are displayed in one or two lines. For that reason, variable voltage 0-Vdd is applied on pin marked as Vee. Trimmer potentiometer is usually used for that purpose. Some versions of displays have built in backlight (blue or green diodes). When used during operating, a resistor for current limitation should be used (like with any LE diode).

LCD Memory

There are three memory blocks inside the display:

- DDRAM Display Data RAM
- CGRAM Character Generator RAM
- CGROM Character Generator ROM

DDRAM Memory

DDRAM memory is used for storing characters that should be displayed. The size of this memory is sufficient for storing 80 characters. One part of these locations is directly connected to the characters on display.

All functions quite simply: it is sufficient to configure display so that addresses are automatically incremented (shift right). Afterwards it sets starting value for the message that should be displayed (for example 00 hex).

After that, all characters sent through lines D0-D7 will be displayed as a message we are used to- from left to right. In this case, displaying starts from the first character in the first line on display since the address is 00 hex. If more than 16 characters are sent, they all will be also memorized but not visible. In order to display them, a shift command should be used. Virtually, everything looks as if LCD display is a "window" which moves left-right over memory locations with characters. In reality, that is how the affect of message "moving"on the screen is obtained (from left to right or vice versa).

If cursor is on, it will appear at location which is currently addressed. In other words, characters will appear at cursor's position while the cursor is automatically moved to the next addressed location. Since this is a sort of RAM memory, data can be written to and read from it. Disadvantage is that the contents will be lost forever upon the power is off.

CGROM Memory

A "map" with all characters that can be displayed are written by default. Each character has corresponding location. Addresses of CGROM memory locations match standard ASCII values of characters. It means that if in a program being currently executed by the microcontroller is written "send letter P to port", the binary value 0101 0000 will appear on the port. This value is ASCII equivalent to the letter P. When this binary number is sent to LCD, a symbol stored on 0101 0000 location in CGROM will be displayed. In other words, the letter "P" will be displayed. This applies to all alphabet letters (upper- and lowercase), but not to numbers!

If one carefully looks at the "map" with characters in this memory, it can be seen that addresses of all digits are "shifted" by 48 in comparison to the values of these digits (address of the digit 0 is 48, of digit 1 is 49, of digit 2 is 50 etc.). For that reason and in order to display digits correctly, each of them needs to be added a decimal number 48 prior to being sent to LCD.

CGRAM Memory

Besides being able to display all standard characters, the LCD can display symbols that user defines on its own. It enables displaying cyrillic fonts as well as many other symbols which fit to the frame of 5x8 dots size. RAM memory (CGRAM) in size of 64 bytes enables the above.

The size of registers of this memory is a standard one (8 bits), but only 5 lower bits are in use. Logic one (1) in every register represents a dimmed dot, while 8 locations considered jointly represent one character. Symbols are usually defined at the beginning of a program by simple writing zeros and units to registers of CGRAM memory so that they form desirable shapes. In order to display them it is sufficient to specify their address.

Interfacing 16*2 LCD with AT89S51 microcontroller

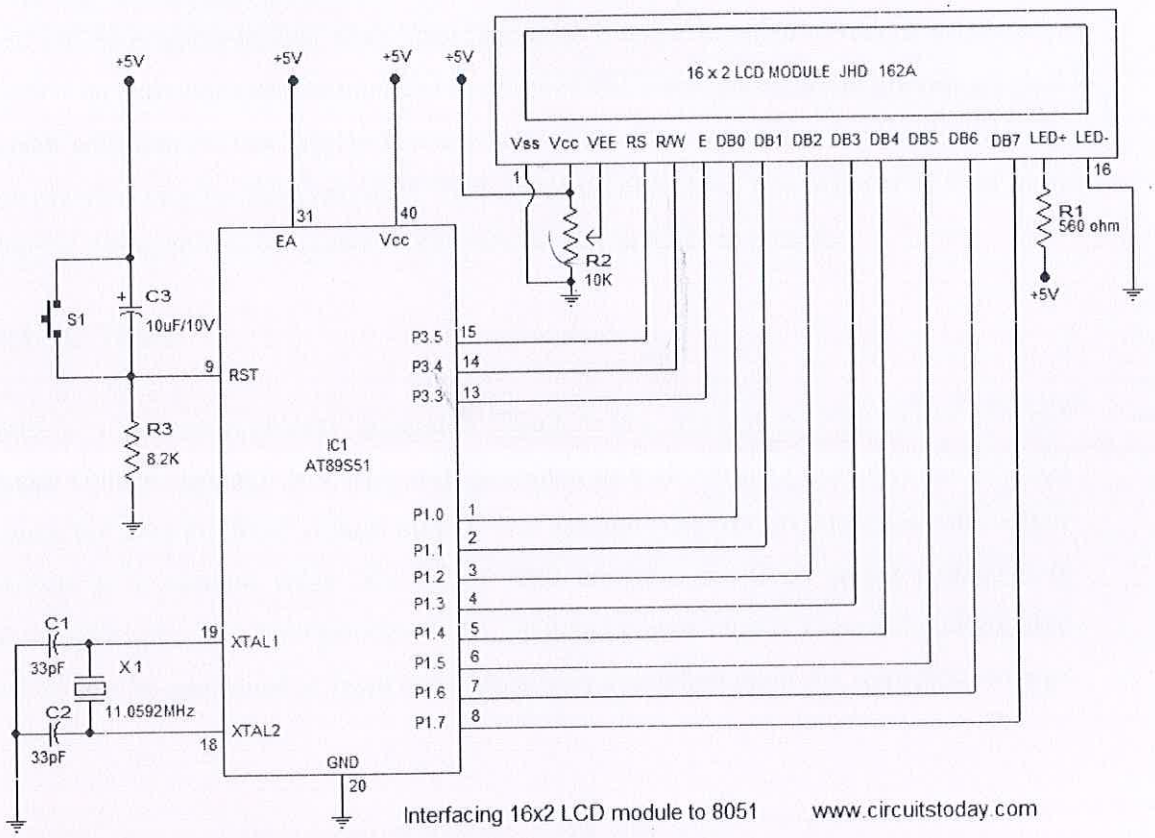


Figure 13: LCD interfaced with AT89S51 Microcontroller

Depending on how many lines are used for connection to the microcontroller, there are 8-bit and 4-bit LCD modes. The appropriate mode is determined at the beginning of the process in a phase called "initialization". In the first case, the data are transferred through outputs D0-D7 as it has been already explained. In case of 4-bit LED mode, for the sake of saving valuable I/O pins of the microcontroller, there are only 4 higher bits (D4-D7) used for communication, while other may be left unconnected. Consequently, each data is sent to LCD in two steps: four higher bits are sent first (that normally would be sent through lines D4-D7), four lower bits are sent afterwards. With the help of initialization,

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Acc. No. SP09096
JUIT, Waknaghat Solan (H.P.)

LCD will correctly connect and interpret each data received. Besides, with regards to the fact that data are rarely read from LCD (data mainly are transferred from microcontroller to LCD) one more I/O pin may be saved by simple connecting R/W pin to the Ground. Such saving has its price. Even though message displaying will be normally performed, it will not be possible to read from busy flag since it is not possible to read from display. LCD is an extremely slow component because of that it was necessary to provide a signal which will indicate that display is ready to receive a new data or a command following the previous one has been executed. That signal is called busy flag and can be read from line D7. When the bit BF is cleared (BF=0), display is ready to receive.

3.3 IC 7805

7805 is a **voltage regulator** integrated circuit. It is a member of 78xx series of fixed linear voltage regulator ICs. The voltage source in a circuit may have fluctuations and would not give the fixed voltage output. The **voltage regulator IC** maintains the output voltage at a constant value. The xx in 78xx indicates the fixed output voltage it is designed to provide. 7805 provides +5V regulated power supply. Capacitors of suitable values can be connected at input and output pins depending upon the respective voltage levels.

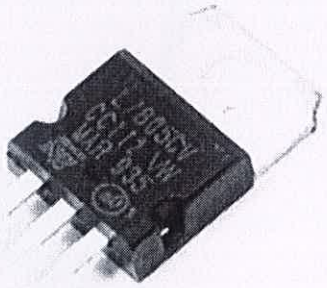

Figure 14 : IC 7805

Pin No	Function	Name
1	Input voltage (5V-18V)	Input
2	Ground (0V)	Ground
3	Regulated output; 5V (4.8V-5.2V)	Output

Table 6: Pin description

3.4 Zigbee Transceiver

The XBee (ZigBee) Module provides an alternative way to transfer data without the use of wires. XBee transceiver is developed by Digi. XBee was among the first transceivers that hit the market and came in a convenient to use casing. The XBee (ZigBee) uses a wireless 2.4GHz transceiver to communicate with another XBee (ZigBee) module. Furthermore, XBee (ZigBee) modules are capable of communicating with more than one XBee (ZigBee) module. Thus, it means you can create a network of XBee modules all over the place as long as they are in range, of course.

Figure 15: Xbee

Some features of XBee are:

- 802.15.4 Protocol created by the IEEE foundation.
- Data rate of 250KBps (Kilobits per second).
- Can be used indoors and outdoors.
- Range is from 100ft-300 for standard XBee modules and 300ft-1 Mile for XBee Pro Modules (depending on where it's used and the line of sight from one XBee to the next XBee).
- The standard XBee has a 1mW transmit power and the XBee Pro has a 60mW transmit power.
- No configuration is required out of the box.
- Default baud rate is 9600bps.

Pin Description

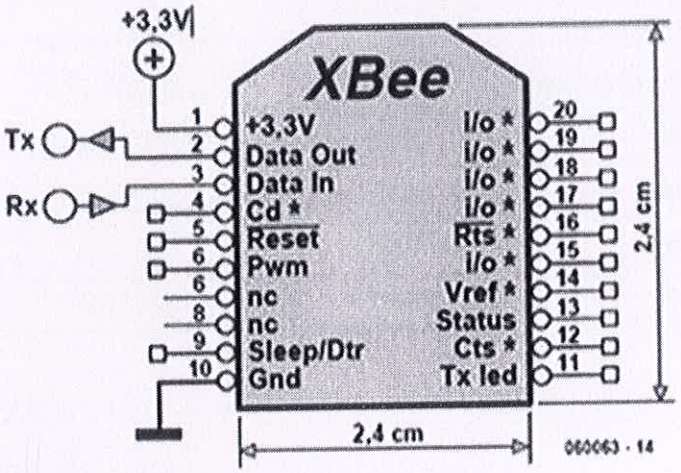

Figure 16: Pin Diagram

For the data transmission & reception only pin 1 (supply), pin 2 (transmit), pin 3 (receive) and pin 10 (ground) are required.

Pin #	Name	Direction	Description
1	VCC	-	Power supply
2	DOUT	Output	UART Data Out
3	DIN / $\overline{\text{CONFIG}}$	Input	UART Data In
4	DO8*	Output	Digital Output 8
5	$\overline{\text{RESET}}$	Input	Module Reset (reset pulse must be at least 200 ns)
6	PWM0 / RSSI	Output	PWM Output 0 / RX Signal Strength Indicator
7	PWM1	Output	PWM Output 1
8	[reserved]	-	Do not connect
9	$\overline{\text{DTR}}$ / SLEEP_RQ / DI8	Input	Pin Sleep Control Line or Digital Input 8
10	GND	-	Ground
11	AD4 / DIO4	Either	Analog Input 4 or Digital I/O 4
12	$\overline{\text{CTS}}$ / DIO7	Either	Clear-to-Send Flow Control or Digital I/O 7
13	ON / $\overline{\text{SLEEP}}$	Output	Module Status Indicator
14	VREF	Input	Voltage Reference for A/D Inputs
15	Associate / AD5 / DIO5	Either	Associated Indicator, Analog Input 5 or Digital I/O 5
16	$\overline{\text{RTS}}$ / AD6 / DIO6	Either	Request-to-Send Flow Control, Analog Input 6 or Digital I/O 6
17	AD3 / DIO3	Either	Analog Input 3 or Digital I/O 3
18	AD2 / DIO2	Either	Analog Input 2 or Digital I/O 2
19	AD1 / DIO1	Either	Analog Input 1 or Digital I/O 1
20	AD0 / DIO0	Either	Analog Input 0 or Digital I/O 0

Table7: Functions of pins of Zigbee

3.5 FT232RL

The FT232RL is a USB Full Speed to Serial UART IC that includes an Oscillator and EEPROM and is available in package(s): 28-Pin SSOP.

The FT232RL is currently sourced by Future Technology Devices International (FTDI Chip).

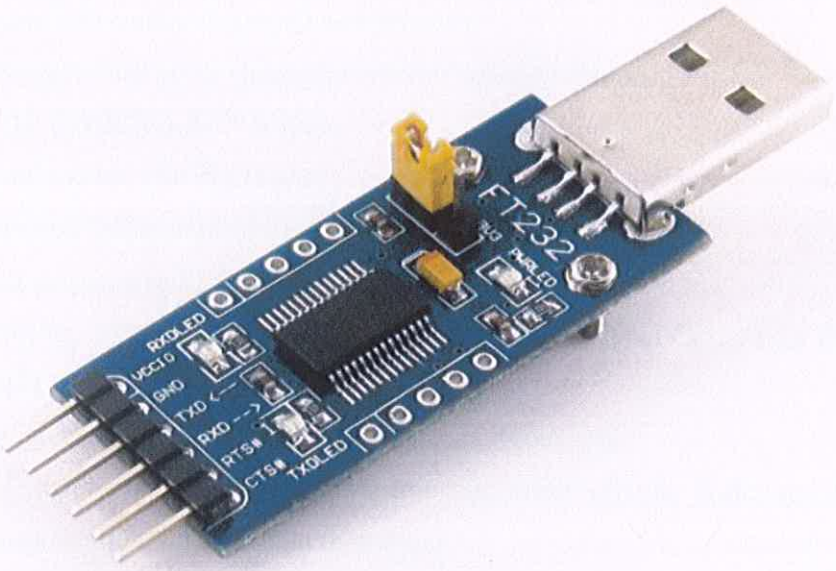

Figure 17: FT232RL

FT232RL Features

- Single chip USB to asynchronous serial data transfer interface.
- Entire USB protocol handled on the chip - No USB-specific firmware programming required.
- UART interface support for 7 or 8 data bits, 1 or 2 stop bits and odd / even / mark / space / no parity.
- Fully assisted hardware or X-On / X-Off software handshaking.
- Data transfer rates from 300 baud to 3 Mega baud (RS422 / RS485 and at TTL levels) and 300 baud to 1 Mega baud (RS232).
- In-built support for event characters and line break condition.
- New USB FTDIChip-ID™ feature.
- New configurable CBUS I/O pins.
- Auto transmit buffer control for RS485 applications.
- Transmit and receive LED drive signals.
- New 48MHz, 24MHz,12MHz, and 6MHz clock output signal Options for driving external MCU or FPGA.
- FIFO receive and transmit buffers for high data throughput.
- 256 Byte receive buffer and 128 Byte transmit buffer utilizing buffer smoothing technology to allow for high data throughput.
- Adjustable receive buffer timeout.
- Synchronous and asynchronous bit bang mode interface options with RD
- and WR
- strobes.
- New CBUS bit bang mode option.
- Integrated 1024 bit internal EEPROM for I/O configuration and storing USB VID, PID, serial number and product description strings.
- Device supplied preprogrammed with unique USB serial number.
- Support for USB suspend / resume.
- Support for bus powered, self powered, and high-power bus powered USB configurations.

- Integrated 3.3V level converter for USB I/O .
- Integrated level converter on UART and CBUS for interfacing to 5V - 1.8V Logic.
- True 5V / 3.3V / 2.8V / 1.8V CMOS drive output and TTL input.
- High I/O pin output drive option.
- Integrated USB resistors.
- Integrated power-on-reset circuit.
- Fully integrated clock - no external crystal, oscillator, or resonator required.
- Fully integrated AVCC supply filtering - No separate AVCC pin and no external R-C filter required.
- UART signal inversion option.
- USB bulk transfer mode.
- 3.3V to 5.25V Single Supply Operation.
- Low operating and USB suspend current.
- Low USB bandwidth consumption.
- UHCI / OHCI / EHCI host controller compatible.
- USB 2.0 Full Speed compatible.
- -40°C to 85°C extended operating temperature range.
- Available in compact Pb-free 28 Pin SSOP and QFN-32 packages (both RoHS compliant).

3.6 Power Supply

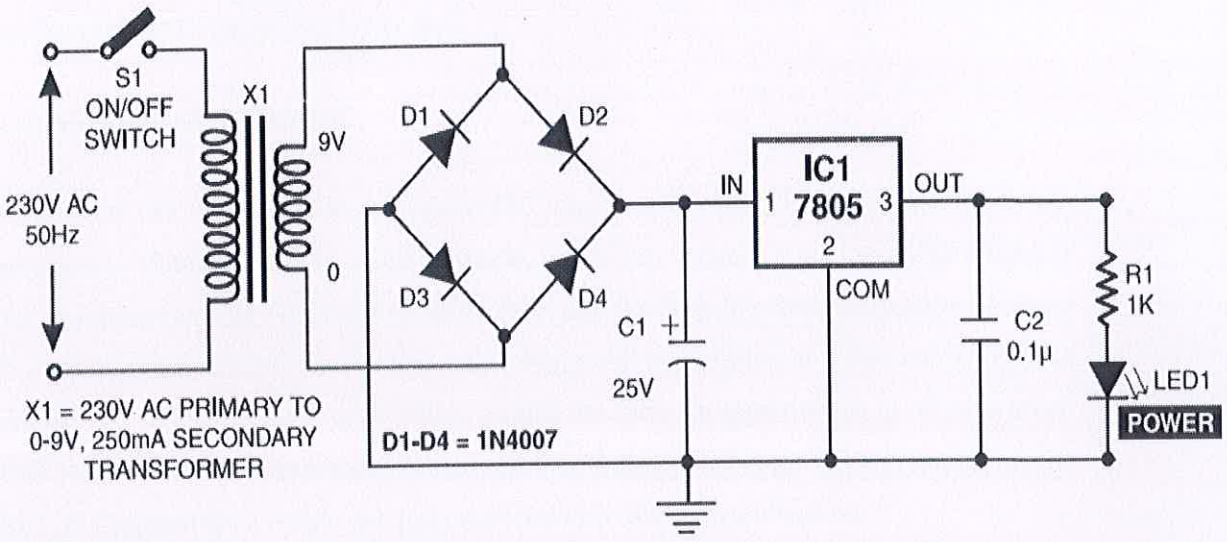

Figure 18: Power Supply

To provide a useable low voltage the Power Supply Unit needs to do a number of things:-

- Reduce the Mains AC (Alternating current) voltage to a lower level.
- Convert this lower voltage from AC to DC (Direct current)
- Regulate the DC output to compensate for varying load (current demand)
- Provide protection against excessive input/output voltages.

Reduction of AC Mains

This is achieved by using a device known as a Transformer an electromagnetic device consisting of an ferrous iron core which has a large number of turns of wire wound

around it, known as the Primary Winding. The ends of these turns of wire being connected to the input voltage (in this case Mains AC). A second number of turns of wire are wound around the Primary Winding, this set being known as the Secondary Winding. The difference between the number of turns provides us with a way of reducing (in our case) a high AC voltage to a lower one.

Conversion of AC to DC

To convert our now low AC voltage to DC we use a Rectifier Diode connected to the Secondary Winding. This is a silicon diode, which has operation analogous to a bicycle tyre valve (as the valve only allows air to flow into the tyre, the diode only allows current to flow in one direction) As our low AC voltage will be working at a frequency of 50Hz (Mains AC frequency) it is desirable to reduce the inherent hum on this to a lower level. This is achieved by a technique known as Smoothing ("Ironing" out the bumps in the AC). A simple way to reduce the hum is to use Full Wave Rectification.

Regulation of output voltage

The Electrolytic Capacitor is a device capable of storing energy the amount of energy and the time it remains stored depending on the value. In a simple PSU the easiest way to provide regulation to compensate for varying load conditions is to use a pair of relatively high value Electrolytic Capacitors. Their values in this case being in the region of 470uF to 2000uF depending on the application and the amount of current required from the output of the unit. One of these capacitors is connected across the DC output of the rectifier diode(s) or bridge, this capacitor also providing an extra degree of smoothing the output waveform. The second capacitor is connected via a low value, medium to high wattage resistor, which assists in limiting the current demand.

Protection against excessive voltages

In a simple PSU the easiest way to do this is by providing fuses at the input to the transformer, generally in the live side of the mains supply, also at the DC outputs. In the

event of an excessive input voltage, or excessive current being drawn from the output, one of these fuses should normally blow protecting the PSU and the equipment connected to it. The transformer may also be fitted with an internal or external thermal fuse, which will open if the transformer becomes hot due to the aforementioned conditions.

CONCLUSION

Today's world is becoming technologically strong and advanced with each passing day. Manual paper work is being eliminated at every sphere of life , be it at work or home. Electronic Notice boards have revolutionized the way of spreading information amongst the crowd. Organizations have started using electronic notice boards for displaying notices and other important information. Even advertisements are being displayed digitally using LEDs at road junctions, crossings and shopping malls. In railway station and bus stands everything from ticket information to platform number etc is displayed on digital moving displays .

Another aspect which is highly eminent nowadays is Data Security.Data can be easily hacked or copied which reduces the quality of communication and increases the risk of information leak.

In this project we see electronic notice boards which store particular information and displays the particular information only till it is provided with new information. It is not stored permanently .

The outcome of this project is an embedded system providing wireless transmission from one point to the other via zigbee transceivers. This system is a reliable and fast medium for data transmission. Apart from the wide applications already mentioned, it has scope for further enhancements in the field of embedded systems where telecommunication is a vital part of the system and thereby holds the power to change the face of present communication systems.

FUTURE WORK

- Alphanumeric LCD's have a limitation on size as well as no of characters. They can be replaced with large LED display boards which are not only eye catching but display characters in a moving fashion one after the other.

- A commercial model should be able to display more than one message at a time. Currently in our project we are using onboard RAM memory to save a single message. To overcome this shortcoming we can interface an EEPROM to save messages. This not only allows more than one message to be displayed at a time but also allows to retrieve messages from the EEPROM even after a power failure.

- In our project we have connected one receiver with the transmitter but zigbee can have up to 32000 nodes so we can connect more than one receiver with a single transmitter. This can have application in colleges or other institution where the receivers can be positioned at various locations according to the need such as hostels, academics and offices.

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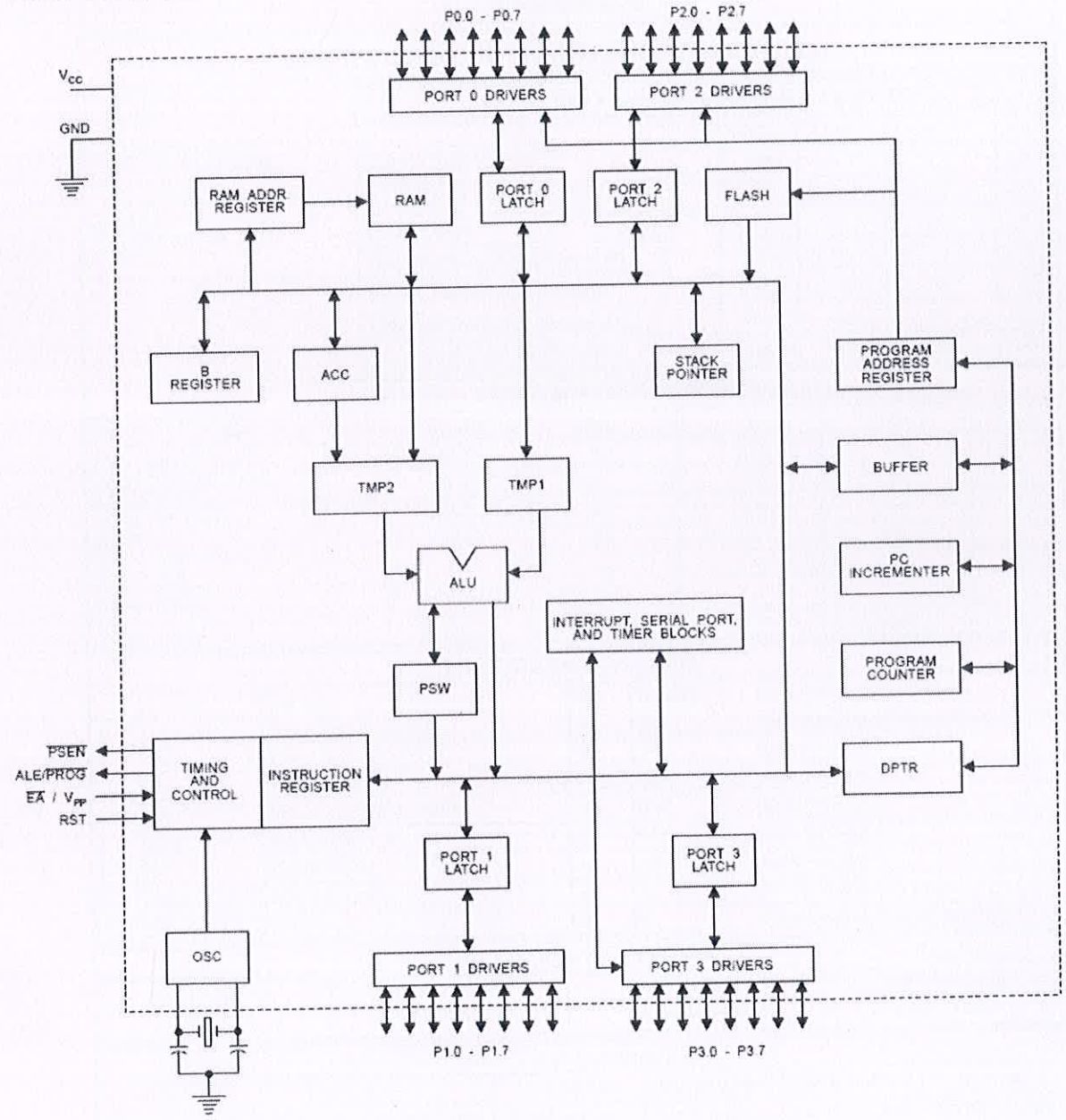
APPENDIX

Block Diagram



Datasheet of LCD (16*2)

www.p-tec.net
sales@p-tec.net

Tel: (719) 589 3122
Fax: (719) 589 3592

PC1602A-L (16x2) Character LCD Display

Features

- **16 Character, 2 Line**
- View Angle 12H or 6H
- TN or STN Fluid
- **Extended Temperature Range available**
- Several Character Types available
- LED or EL Backlight available

Absolute Maximum Ratings at T_A = 25 °C

Item	Symbol	Min	Max	Unit
Power Supply (Logic)	Vdd	-0.3	7.0	V
Power Supply (LCD)	Vo	Vdd -0.3	Vdd 12.0	V
Input Voltage	Vi	- 0.3	Vdd	V
Operating Temperature (Standard)	Topr	0	50	°C
Storage Temperature (Standard)	Tstg	- 20	70	°C
Extended Operating Temperature	Topr	- 20	70	°C
Extended Storage Temperature	Tstg	- 30	80	°C

Electrical Characteristics at T_A = 25 °C, Vdd=5V+0.25V

Item	Symbol	Min	Typ	Max	Unit
Power Supply (Logic)	Vdd-Vss	4.7	5.0	5.3	V
Supply Current	Idd	—	2.0	3.0	mA
LCD Driving Voltage	Vdd -Vo	4.2	4.5	4.8	V
Input Voltage "H"	Vih	2.2	—	Vdd	V
Input Voltage "L"	Vil	—	—	0.6	V
Output Voltage "H"	Voh	2.4	—	—	V
Output Voltage "L"	Vol	—	—	0.4	V

Interface Pin Connection

No	Symbol	Function	No	Symbol	Function
1	Vss	Power Supply (GND)	9	DB2	Data Bus Line 2
2	Vdd	Power Supply (+5V)	10	DB3	Data Bus Line 3
3	Vo	Contrast Adjust	11	DB4	Data Bus Line 4
4	RS	Instruction/Register Select	12	DB5	Data Bus Line 5
5	R/W	Read/Write	13	DB6	Data Bus Line 6
6	E	Enable Signal	14	DB7	Data Bus Line 7
7	DB0	Data Bus Line 0	15	A	Power Supply for LED Backlight (+)
8	DB1	Data Bus Line 1	16	K	Power Supply for LED Backlight (-)

LED Backlight Specifications

Forward Voltage	Forward Current	Power Dissipation	Peak Wavelength
4.2V (Typ)	195mA (Max)	900mW (Max)	570nm (Typ)

Mechanical Specifications

Item	Overall Size	Viewing Area	Character Size	Character Pitch	Dot Size
Specifications	80.0W x 36.0H x 8.8T (BL12.7T)	65.0W x 16.0H	2.96W x 5.56H	3.55W x 5.94H	0.56W x 0.66H

All dimensions are in mm. Tolerance is ± 0.3 Unless otherwise specified

COMMAND	COMMAND CODE										COMMAND CODE	E-CYCLE f_{osc}=250KHz
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
SCREEN CLEAR	0	0	0	0	0	0	0	0	0	1	Screen Clear, Set AC to 0 Cursor Reposition	1.64ms
CURSOR RETURN	0	0	0	0	0	0	0	0	1	*	DDRAM AD=0, Return, Content Changeless	1.64ms
INPUT SET	0	0	0	0	0	0	0	1	I/D	S	Set moving direction of cursor, Appoint if move	40us
DISPLAY SWITCH	0	0	0	0	0	0	1	D	C	B	Set display on/off,cursor on/off, blink on/off	40us
SHIFT	0	0	0	0	0	1	S/C	R/L	*	*	Remove cursor and whole display,DDRAM changeless	40us
FUNCTION SET	0	0	0	0	1	DL	N	F	*	*	Set DL,display line,font	40us
CGRAM AD SET	0	0	0	1	ACG						Set CGRAM AD, send receive data	40us
DDRAM AD SET	0	0	1	ADD							Set DDRAM AD, send receive data	40us
BUSY/AD READ CT	0	1	BF	AC							Executing internal function, reading AD of CT	40us
CGRAM/ DDRAM DATA WRITE	1	0	DATA WRITE								Write data from CGRAM or DDRAM	40us
CGRAM/ DDRAM DATA READ	1	1	DATA READ								Read data from CGRAM or DDRAM	40us
	I/D=1: Increment Mode; I/D=0: Decrement Mode S=1: Shift S/C=1: Display Shift; S/C=0: Cursor Shift R/L=1: Right Shift; R/L=0: Left Shift DL=1: 8D DL=0: 4D N=1: 2R N=0: 1R F=1: 5x10 Style; F=0: 5x7 Style BF=1: Execute Internal Function; BF=0: Command Received										DDRAM: Display data RAM CGRAM: Character Generator RAM ACG: CGRAM AD ADD: DDRAM AD & Cursor AD AC: Address counter for DDRAM & CGRAM	E-cycle changing with main frequency. Example: If fcp or f_{osc}=270KHz 40us x 250/270 =37us

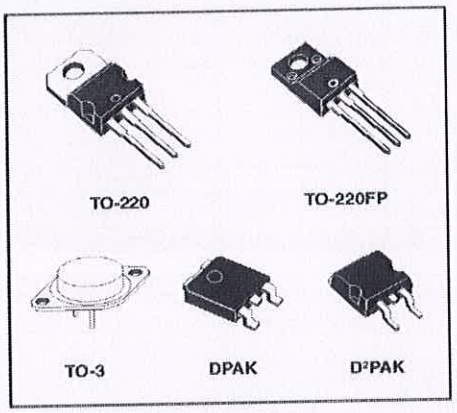
Datasheet of IC 7805

L78xx
L78xxC

Positive voltage regulators

Features

- Output current to 1.5 A
- Output voltages of 5; 6; 8; 8.5; 9; 12; 15; 18; 24 V
- Thermal overload protection
- Short circuit protection
- Output transition SOA protection



Description

The L78xx series of three-terminal positive regulators is available in TO-220, TO-220FP, TO-3, D^2PAK and DPAK packages and several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1 A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltage and currents.

Table 1. Device summary

Part numbers	
L7805	L7809C
L7805C	L7812C
L7806C	L7815C
L7808C	L7818C
L7885C	L7824C

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ELECTRICAL CHARACTERISTICS FOR L7805 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 10V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	4.8	5	5.2	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 8 to 20 V	4.65	5	5.35	V
ΔV_o*	Line Regulation	V_i = 7 to 25 V T_j = 25 °C V_i = 8 to 12 V T_j = 25 °C		3 1	50 25	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			100 25	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 8 to 25 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		0.6		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_O
SVR	Supply Voltage Rejection	V_i = 8 to 18 V f = 120 Hz	68			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

ELECTRICAL CHARACTERISTICS FOR L7806 (refer to the test circuits, T_j = -55 to 150 °C, V_i = 15V, I_o = 500 mA, C_i = 0.33 µF, C_o = 0.1 µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	5.75	6	6.25	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 9 to 21 V	5.65	6	6.35	V
ΔV_o*	Line Regulation	V_i = 8 to 25 V T_j = 25 °C V_i = 9 to 13 V T_j = 25 °C			60 30	mV mV
ΔV_o*	Load Regulation	I_o = 5 to 1500 mA T_j = 25 °C I_o = 250 to 750 mA T_j = 25 °C			100 30	mV mV
I_d	Quiescent Current	T_j = 25 °C			6	mA
ΔI_d	Quiescent Current Change	I_o = 5 to 1000 mA			0.5	mA
ΔI_d	Quiescent Current Change	V_i = 9 to 25 V			0.8	mA
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift	I_o = 5 mA		0.7		mV/°C
eN	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C			40	µV/V_O
SVR	Supply Voltage Rejection	V_i = 9 to 19 V f = 120 Hz	65			dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2	2.5	V
R_o	Output Resistance	f = 1 KHz		19		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_j = 25 °C		0.75	1.2	A
I_{scp}	Short Circuit Peak Current	T_j = 25 °C	1.3	2.2	3.3	A

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

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