JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2024

B.Tech-VI Semester (ECE)

COURSE CODE(CREDITS): 18B11EC612 (4) MAX. MARKS: 35

COURSE NAME: VLSI TECHNOLOGY

COURSE INSTRUCTORS: Dr. Shruti Jain MAX. TIME: 2 Hours

Note: (a) *All questions are compulsory.*

(b)Marks are indicated against each question in square brackets.

(c) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

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SHORT QUESTIONS (10 × 1 = 10) [CO 1, 2, 3]

1.

i. Low noise margin is expressed as _____

ii. For *n*MOS saturated enhancement load inverter biased at V_{DD} = 5V. The transistor parameters are $V_{TOD} = V_{TOL}$ = 0.8V, k_n' = 35μA/ V^2,ν_0 = 0.1V and ν_i = 4.2V. For calculation of high input voltage, load is in_____ region.

iii. For calculation of midpoint voltage, both transistors of inverters are in _____

iv. The MOSFET stands for_____

v. The switching threshold voltage V_{TH} for an ideal inverter is equal to_____

vi. Specify the colors for *n*-diffusion, metal 1 layer, polysilicon and demarcation line in stick diagram.

vii. In general, *p*-MOS in series implement a _____gate. How many *n*-MOS transistors are in logic diagram of NAND 3 gate?

viii. Calculate Logic Swing of a digital logic circuit having the following information: V_{IL} = 0.6V, V_{IH} = 1.5V, V_{OL} = 0.2V and V_{OH} = 1.8V.

ix. In nMOS depletion load inverter configuration depletion mode device is called as _____

x. The enhancement mode n-MOS load inverter requires 2 different supply voltages to keep load transistor in _____ region

LONG QUESTIONS

2.

i. Sita is designing CMOS inverter with the following parameters: V_{Tn} = 0.5V, V_{Tp} = -0.5V, k_n`= 80μA/V$^2$, $k_p$`= 40 μA/V^2 and V_{DD} = 3.5V, $(W/L)_n = (W/L)_p = 2$. Help her in finding input voltage (v_i)when output voltage (v_0) is 3V.

ii. Ananya is designing a NAND 3 gate using CMOS technology with the following parameters: V_{Tn} = 0.5V, V_{Tp} = -0.5V, k_n`= 80μA/V$^2$, $k_p$`= 40 μA/V^2 and V_{DD} = 3.5V, $(W/L)_n = (W/L)_p = 2$. Help her in finding the midpoint voltage for the designed circuit.

[CO4] [5 + 5]

3.

i. Explain the different steps of fabrication for enhancement *n*-type MOSFET

ii. Draw the stick diagram of the logic expression $f(A,B,C)=\overline{A+B(C+D)}$ using CMOS logic. Find the equivalent circuit for *n*MOS transistor only, assuming that $(W/L)_n = (W/L)_p = 10$.

[CO5 [4 + 6]

4. What are pass transistors? Derive *pull up to pull down* ratio if one of the inverter is fed to another inverter through a series of two pass transistors. Assume $V_{th} = 0.2V_{DD}$, $V_{thdep} = -0.6V_{DD}$ and $V_{thp} = 0.3V_{DD}$.

[CO6][5]