JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-3 EXAMINATION- June 2024

B. Tech-VI Semester (ECM)

COURSE CODE(CREDITS): 21B11EM611 (3) MAX. MARKS: 35

COURSE NAME: Computer Organization and Architecture

COURSE INSTRUCTORS: Dr. Naveen Jaglan MAX. TIME: 2 Hours

Note: *(a) All questions are compulsory.*

(b)Marks are indicated against each question in square brackets.

(c) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

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1. Consider a memory hierarchy with a write back cache. The cache has an access time of 25ns. 90% of all the memory accesses are found in the cache itself. The main memory access time is 300ns. The 20% of the cache blocks are dirty. The cache block size is 4 bytes. Calculate the average memory access time?

[CO-1; 4 marks]

2. Convert a hexadecimal number $(2A3B)_H$ into single precision IEEE 754 floating point standard. Explain the algorithm for aligning mantissas and exponent during addition of floating-point numbers. Show the step-by-step addition process when the following floating-point numbers are added:

$$(1.111)_2 \times 2^{-1} + (1.011)_2 \times 2^{-3}$$

[CO-2; 4 marks]

3. Explain the complete process of fetching, decoding and execution of the instruction with the help of instruction cycle state diagram.

[CO-4; 2 marks]

4. What are the differences between interrupt request and DMA request? What are the main differences between DMA Burst Mode and DMA Transparent Modes of data transfer. It is necessary to transfer 256 words from a magnetic disk to a memory section starting from address 1230. The transfer is by means of a DMA:

(a) Give the initial values that the CPU must transfer to the DMA controller.

(b) Give the step-by-step account of the actions taken during the input of the first two words.

[CO-2; 3+2=5 marks]

5. (a) Formulate a six-stage instruction pipeline for a computer. Specify the operations to be performed in each stage. Explain two possible solutions that can be used in the instruction pipeline in order to minimize the pipelining hazards.

(b) A non-pipeline system takes 50ns to process a task. The same task can be processed in a 6-stage pipeline with a clock cycle of 10ns. Determine the speedup ratio of pipeline system for 100 tasks. [CO-3; 3+2=5 marks]

6. (a) What is the difference between Memory Mapped I/O and I/O Mapped I/O. What are the advantages and disadvantages of each?

(b) What hit ratio is required for cache to reduce the effective memory access time from 150 ns to 42 ns if cache access time is 30 ns? [CO-5; 3+2=5 marks]

7. (a) Define the following: (i) Microoperation, (ii) Microinstruction and (iii) Microprogram. What is the main difference between a microprocessor and a microprogram?

(b) A computer system contains a cache. Uncached memory access takes 9 times longer than access to cache. If the cache has a hit ratio of 0.8, calculate the ratio of cached memory access time to uncached memory access time? [CO-4; 3+2=5 marks]

8. (a) The message below coded in the 7-bit Hamming code is transmitted through a noisy channel. Decode the message assuming that at most a single error occurred in the word: 1001001

(b) What is Interrupt driven I/O and interrupt handling mechanism? Explain the main difference between vectored and non-vectored interrupts? [CO-5; 2+3=5 marks]