JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- 2024

B.Tech-VI Semester (ECE)

COURSE CODE(CREDITS): 18B11EC612 (4) MAX. MARKS: 25

COURSE NAME: VLSI TECHNOLOGY

COURSE INSTRUCTORS: Dr. Shruti Jain MAX. TIME: 1 Hour 30 Minutes

Note: *(a)All questions are compulsory.*
(b)Marks are indicated against each question in square brackets.
(c) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

SHORT QUESTIONS (10 × 1 = 10) [CO 1, 2, 3]

1.

i. What is the effect of substrate bias on the linear current of *p*-MOS transistor? State the condition also.

ii. Sita is working on threshold voltage. She comes to know that total voltage comprises different parts. Help her in explaining those parts. (Write all formulas).

iii. Help Shyam in explaining that depth of depletion region is a function of Fermi potential.

iv. What is the effect of linear region on oxide related capacitance?

v. Show diagrammatically length of source, junction depth, depletion depth of source and oxide thickness of *n*-MOS transistor.

vi. Let Abhay know how to calculate area and perimeter for the drain diffusion capacitance.

vii. What is the Fermi potential for depletion mode *n*-substrate and enhancement mode *p*-substrate?

viii. Why the junction capacitance for source and drain are equal? Explain it using equations.

ix. Explain Ansh the different modes of energy band diagram. Explain maximum depth.

x. Help Seema in writing the formulas of permittivity of Silicon, Intrinsic semiconductor concentration, and volt temperature equivalent.

LONG QUESTIONS (3 × 5 = 15)

2. An n-MOS transistor is fabricated with the following physical parameters $N_D = 2\times10^{20}$ cm^{-3}, $N_{A(substrate)} = 10^{15}cm^{-3}$, $W = 10\mu m$, $Y = 6\mu m$, $x_j = 0.5\mu m$, $t_{ox} = 0.05\mu m$, $V_{to} = 0.8V$, $N_{Asw} = 16 \times10^{15}$ cm^{-3}. Find the effective drain parasitic capacitance for abrupt junction when the drain node voltage is 2.5V. Assume $C_{jo} = 9.6 \times 10^{-9}$ F/cm^2, and $C_{josw} = 36.94 \times 10^{-9}$ F/cm^2 [5, CO3]

3.

a) The current in an enhancement mode *n*MOS transistor biased in saturation mode was measured to be 1 mA at a drain source voltage of 5V. When the drain source voltage was increased to 6V while keeping gate source voltage same. The drain current increased to 1.02 mA. Assume that drain to source saturation voltage is much smaller than the applied drain source voltage. Evaluate the channel length modulation parameter λ (in V^{-1}).

b) In a technology for which the gate oxide thickness is 20nm, find the value of N_A, for which $\gamma = 0.5V^{1/2}$. (b) If the doping level is maintained but the gate oxide thickness is increased to 100nm, what does γ become? [2 + 1.5 + 1.5, CO1]

4.

a) Consider an *n*-channel MOSFET with $t_{ox} = 20nm$, $\mu_n = 650cm^2$/ V-s, $V_{th} = 0.8V$ and $W/L = 10$. Find the drain current $V_{GS} = 2V$ and $V_{DS} = 1.2V$.

b) In the circuit shown n Fig 1. For the MOS transistors, $\mu_n C_{ox} = 100\ \mu A/V^2$ and the threshold voltage $V_{th} = 1$ V. The voltage V_x at the source of the upper transistor is____

_____

c) The drain of an *n* – channel MOSFET is shorted to the gate. The threshold voltage of MOSFET is 1 V. If the drain current is 1 mA for $V_{GS} = 2$ V, then for $V_{GS} = 3$ V, I_D is

_____ [1 + 2 + 2, CO2]

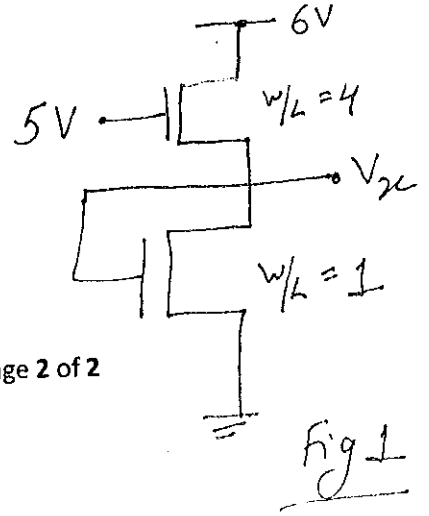

Fig 1