JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-2 EXAMINATION- 2024

B. Tech-VI Semester (ECM)

COURSE CODE(CREDITS): 21B11EM611 (3) MAX. MARKS: 25

COURSE NAME: Computer Organization and Architecture

COURSE INSTRUCTORS: Dr. Naveen Jaglan MAX. TIME: 1 Hour 30 Minutes

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Note: *(a) All questions are compulsory.*

(b)Marks are indicated against each question in square brackets.

(c) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

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1. Show the step-by-step restoring division process for signed numbers when the following binary numbers are divided:

(-18) ÷ (3)

Assume 6-bit registers that hold the signed and unsigned numbers.

[CO-1; 4 marks]

2. Convert a hexadecimal number $(2A3B)_H$ into single precision IEEE 754 floating point standard. Explain the algorithm for aligning mantissas and exponent during addition of floating-point numbers. Show the step-by-step addition process when the following floating-point numbers are added:

$(1.111)_2 \times 2^{-1} + (1.011)_2 \times 2^{-3}$

[CO-2; 4 marks]

3. The access time of a cache memory is 100 ns and that of main memory 1000 ns. It is estimated that 80 percent of the memory requests are for read and the remaining 20 percent for write. The hit ratio for read accesses only is 0.9. A write through procedure is used.

(a) What is the average access time of the system considering only memory read cycles?
(b) What is the average access time of the system considering only memory write cycles?
(c) What is the average access time of the system for both read and write requests?
(d) What is the effective hit ratio taking into consideration the write cycles?

[CO-3; 4 marks]

4. Explain the complete process of fetching, decoding and execution of the instruction with the help of instruction cycle state diagram.

[CO-4; 3 marks]

5. Write one main difference between:

(a) RISC and CISC Processor
(b) Computer Organization and Computer Architecture
(c) Von Neumann and Harvard Architecture
(d) Direct and Indirect Addressing Modes
(e) Spatial Locality and Temporal Locality

[CO-2; 5 marks]

6. What are the advantages of set-associative cache mapping techniques over direct mapping techniques? Consider a computer system with main memory address of 36-Bits, Cache memory size of 256 KB and block size of 64 bytes. Calculate the number of Tag bits in direct mapping, 4-way set associative mapping and Fully-associative mapping.

[CO-3; 2+3 = 5 marks]