JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-1 EXAMINATIONS-FEBRUARY-2024

B.Tech-VI Semester (ECE)

COURSE CODE (CREDITS): 18B11EC612 (4)   MAX. MARKS: 15

COURSE NAME: VLSI Technology

COURSE INSTRUCTOR: Dr. Pardeep Garg   MAX. TIME: 1 Hour

Note: *(a) All questions are compulsory. (b) Carrying of mobile phone during examinations will be treated as case of unfair means. (c) Marks are indicated against each question in square brackets. (d) The candidate is allowed to make suitable numeric assumptions wherever required for solving problems.*

Q1. Starting with the initial concept, how does the idea finally reach to a finished Very Large Scale Integration (VLSI) chip designing; discuss the steps involved in this whole process with the help of a design hierarchy.   **(CO-2, 2 marks)**

Q2. Discuss the concept of Moore's Law in the context of VLSI.   **(CO-2, 2 marks)**

Q3. Discuss the significance of 'Complementary' in Complementary Metal-Oxide Semiconductor (CMOS) with proper justification.   **(CO-3, 1 mark)**

Q4. Realize the following switching function using CMOS logic (in one circuit) assuming that the inputs (x, y, z) are available in uncomplemented form only.   **(CO-4, 3 marks)**

$$f(x, y, z) = \bar{x}.\bar{y} + x.y.\bar{z}$$

Q5. Show the realization of 'Sum' output of a Half-Adder circuit using CMOS logic (in one circuit) assuming that the inputs are available in uncomplemented form only.   **(CO-4, 3 marks)**

Q6. Discuss the importance of a transmission gate (TG) in VLSI.   **(CO-3, 1 mark)**

Q7. Draw the circuit to design a 2-input XNOR gate using Transmission Gate (TG) and explain its functioning in detail.   **(CO-3, 3 marks)**