JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST-3 EXAMINATION- DEC 2023

B. Tech-V Semester (CSE/IT)

COURSE CODE(CREDITS):18B11CI514(3) MAX. MARKS: 35

COURSE NAME: Computer Organization and Architecture

COURSE INSTRUCTORS: Dr. Naveen Jaglan, Dr. Harsh Sohal, Dr. Alok Kumar and Mr. Munish Sood MAX. TIME: 2 Hours

---

Note: *(a) All questions are compulsory.*

(b)Marks are indicated against each question in square brackets.

(c) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

---

1. Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied:

(-9) × (-10)

Assume 5-bit registers that hold the signed numbers. [CO-1; 4 marks]

2. Convert a hexadecimal number $(2A3B)_H$ into single precision IEEE 754 floating point standard. Explain the algorithm for aligning mantissas and exponent during addition of floating-point numbers. Show the step-by-step addition process when the following floating-point numbers are added:

$(1.111)_2 \times 2^{-1} + (1.011)_2 \times 2^{-3}$ [CO-2; 4 marks]

3. Explain the complete process of fetching, decoding and execution of the instruction with the help of instruction cycle state diagram. [CO-4; 2 marks]

4. What are the differences between interrupt request and DMA request? What are the main differences between DMA Burst Mode and DMA Transparent Modes of data transfer. It is necessary to transfer 256 words from a magnetic disk to a memory section starting from address 1230. The transfer is by means of a DMA:
(a) Give the initial values that the CPU must transfer to the DMA controller.
(b) Give the step-by-step account of the actions taken during the input of the first two words.
[CO-2; 3+2=5 marks]

5. (a) Formulate a six-stage instruction pipeline for a computer. Specify the operations to be performed in each stage. Explain two possible solutions that can be used in the instruction pipeline in order to minimize the pipelining hazards.

(b) A non-pipeline system takes 50ns to process a task. The same task can be processed in a 6-stage pipeline with a clock cycle of 10ns. Determine the speedup ratio of pipeline system for 100 tasks. [CO-3; 3+2=5 marks]

6. (a) What is the difference between Memory Mapped I/O and I/O Mapped I/O. What are the advantages and disadvantages of each?

(b) The system bus can be used by one module at a time, how the contest for the system bus can be resolved by Daisy Chain Method arbitration scheme? What are the advantages and disadvantages of this scheme? [CO-5; 3+2=5 marks]

7. (a) Define the following: (i) Microoperation, (ii) Microinstruction and (iii) Microprogram. What is the main difference between a microprocessor and a microprogram?

(b) What is Cache Coherence, and why is it important in shared memory multiprocessor systems? How can the problem be resolved with a snoopy cache controller? [CO-4; 3+2=5 marks]

8. (a) The message below coded in the 7-bit Hamming code is transmitted through a noisy channel. Decode the message assuming that at most a single error occurred in each word: 1001001,0111001,1110110,0011011.

(b) What is Interrupt driven I/O and interrupt handling mechanism? Explain the main difference between vectored and non-vectored interrupts? [CO-5; 2+3=5 marks]