JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- 2023

B.Tech-III Semester (ECE)

COURSE CODE (CREDITS): 18B11EC312(4) MAX. MARKS: 25

COURSE NAME: Digital Electronics and Logic design

COURSE INSTRUCTORS: Munish Sood MAX. TIME: 1 Hour 30 Minutes

Note: (a)*All questions are compulsory.*

(b)Marks are indicated against each question in square brackets.

(c) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

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Q1) Two 4 Bit numbers (1101 and 1011) are applied to a 4 bit parallel adder. The input carry is 1. Determine the sum and the output carry. Show the result using suitable Block diagram.

[5] CO-3

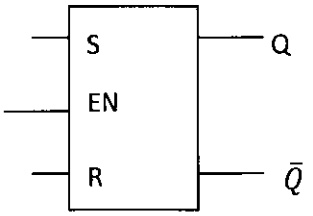
Q2) a) Determine the Logic required to decode the binary number 1011 by producing a HIGH level on the output. **[3] CO-3, CO-4**

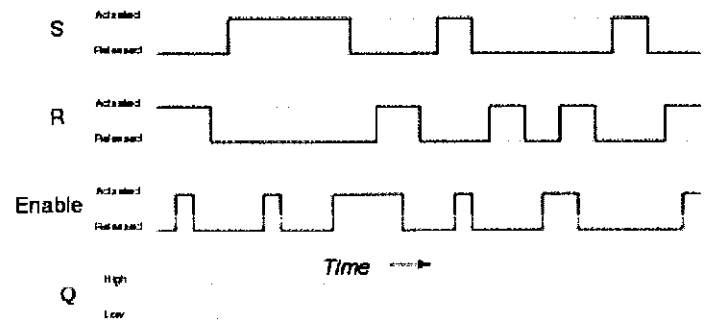
b) A 3-line to 8-line decoder can be used for octal to decimal decoding. When a binary 101 is on the inputs, which output is activated? **[2] CO-3**

Q3) a) Convert the Gray code 1011 to binary with exclusive OR gates. **[2] CO-4**

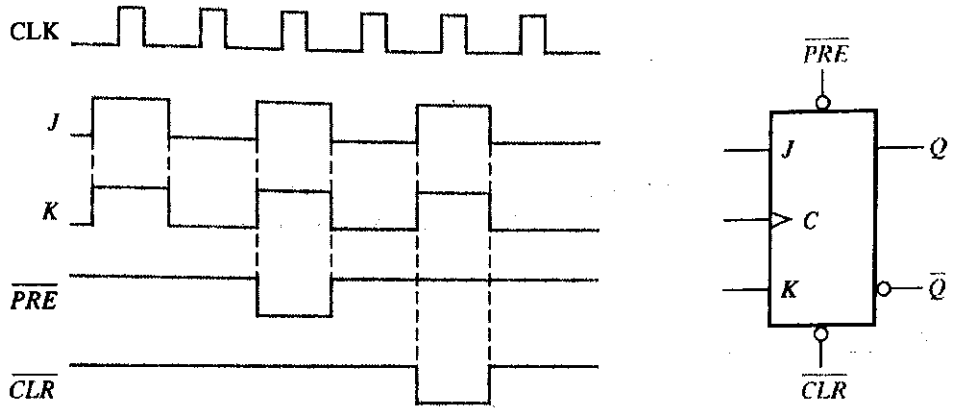
b) Draw the logic diagram for converting an 8 bit binary number to Gray Code. **[4] CO-3**

Q4) For a gated S-R latch, determine the Q output. Assume that Q is initially LOW. [3] CO-3





Q5) Determine the Q waveform relative to the clock if the signals shown are applied to the inputs of the J-K flip flop. Assume that Q is initially LOW. **[4] CO-3, CO-5**



Q6) Find out the characteristic equation and excitation table of J-K flip flop using characteristic table of J-K flip flop. **[5] CO-3,CO-5**